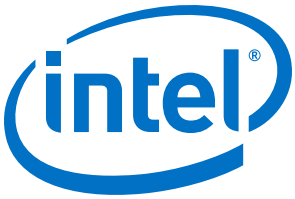
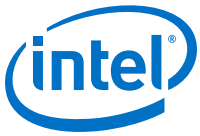


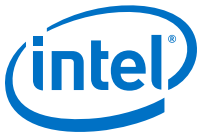
Intel® Xeon® Processor E5-1600, E5-2600, and E5-4600 v3 Product Families, Volume 1 of 2, Electrical

Datasheet

June 2015

Order No.: 330783-002

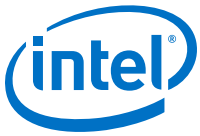




Revision History

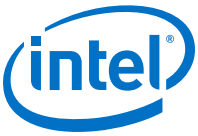
Document Number	Revision Number	Description	Date
330783	001	Initial release	September 2014
330783	002	Added Intel® Xeon® Processor E5-4600 v3 Product Families.	June 2015

Contents



Figures

Tables



1.0 Introduction

The Datasheet provides descriptions of the Intel® Xeon® processor v3 product families registers and Electrical specifications (including DC electrical specifications, signal integrity, and land and signal definitions).

This document is distributed as a part of the complete Datasheet consisting of two volumes.

Note: Unless specified otherwise, the term "Intel® Xeon® processor v3 product families", "server processor", or "processor" will represent the following processors throughout the rest of the document. Features within this document may not be supported on all processor types and SKUs.

This document covers the following processors:

- Intel® Xeon® processor E5-1600 and E5-2600 v3 product families; for Efficient Performance Server, Workstation, HPC, Storage and Embedded.
- Intel® Core™ i7-5960X Extreme Edition Processor; For High-End Desktop (HEDT).

The Intel® Xeon® processor v3 product families is the next generation of 64-bit, multi-core enterprise processor built on 22-nm process technology. Based on the low power / high performance processor microarchitecture, the processor is designed for a platform consisting of a processor and the Platform Controller Hub (PCH).

Note: Some processor features are not available on all platform segments, processor types, and processor SKUs.

The processor supports up to 46 bits of physical address space and 48-bit of virtual address space.

- The Intel® Xeon® processor E5-1600 and E5-2600 v3 product families and Intel® Xeon® processor E5-4600 v3 product families feature (per socket) two Intel® QuickPath Interconnect point-to-point links capable of up to 9.6 GT/s, up to 40 lanes of PCI Express* 3.0 links capable of 8.0 GT/s, and 4 lanes of DMI2/PCI Express* 2.0. It features 2 IMCs (Integrated Memory Controller), which support DDR4 DIMMs.

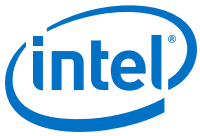
Included in this family of processors is an integrated memory controller (IMC) and an integrated I/O (IIO) on a single silicon die. This single die solution is known as a monolithic processor.

For supported processor configurations, refer to:

- *Intel® 64 and IA-32 Architectures Software Developer's Manuals*

1.1 Electrical Datasheet Introduction

This is volume one (Vol 1) of the processor Datasheet, which provides DC electrical specifications, signal integrity, differential signaling specifications, and land and signal definitions of the processor.



Additionally, this document may be used by system test engineers, board designers, and BIOS developers.

1.1.1 Structure and Scope

The following table summarizes the structure and scope of each volume of the processor Datasheet.

Table 1. Structure of the Processor Datasheet

Volume One: Electrical Datasheet
• Introduction
• Electrical Specifications
• Processor Land Listing
• Processor Signal Descriptions
Volume Two: Register Information
• Configuration Process and Registers Overview
• Configuration Space Registers (CSR)
• Model Specific Registers (MSR)

1.1.2 Related Publications

Refer to the following documents for additional information.

Table 2. Public Publications

Document	Document Number/Location
Advanced Configuration and Power Interface Specification 4.0	http://www.acpi.info/
PCI Local Bus Specification 3.0	http://www.pcisig.com/
PCI Express Base Specification, Revision 3.0	http://www.pcisig.com/
PCI Express Base Specification, Revision 2.1	
PCI Express Base Specification, Revision 1.1	
PCIe Gen 3 Connector High Speed Electrical Test Procedure*	325028-001 / http://www.intel.com/content/www/us/en/io/pci-express/pci-express-architecture-devnet-resources.html
Connector Model Quality Assessment Methodology	326123-002 / http://www.intel.com/content/www/us/en/architecture-and-technology/intel-connector-model-paper.html
DDR4 SDRAM Specification and Register Specification	http://www.jedec.org/
Intel® 64 and IA-32 Architectures Software Developer's Manuals • *Volume 1: Basic Architecture* • *Volume 2A: Instruction Set Reference, A-M* • *Volume 2B: Instruction Set Reference, N-Z* • *Volume 3A: System Programming Guide*	325462 / http://www.intel.com/products/processor/manuals/index.htm

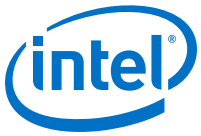
continued...

Document	Document Number/Location
• *Volume 3B: System Programming Guide* *Intel® 64 and IA-32 Architectures Optimization Reference Manual*	
Intel® Virtualization Technology Specification for Directed I/O Architecture Specification	http://www.intel.com/content/www/us/en/intelligent-systems/intel-technology/vt-directed-io-spec.html
Intel® Trusted Execution Technology Software Development Guide	http://www.intel.com/technology/security/

1.1.3 Terminology

Term	Description
ASPM	Active State Power Management
BMC	Baseboard Management Controller
Cbo	Caching Agent (also referred to as CA). It is a term used for the internal logic providing ring interface to LLC and Core. The Cbo is a functional unit in the processor. A Caching Agent is defined per the *RS - Intel® QuickPath Interconnect External Link Specification*.
DDR4	Fourth generation Double Data Rate SDRAM memory technology.
DMA	Direct Memory Access
DMI2	Direct Media Interface Gen2 operating at PCI Express 2.0 speed.
DSB	Data Stream Buffer. Part of the processor core architecture.
DTLB	Data Translation Look-aside Buffer. Part of the processor core architecture.
DTS	Digital Thermal Sensor
ECC	Error Correction Code
Enhanced Intel SpeedStep® Technology	Allows the operating system to reduce power consumption when performance is not needed.
Execute Disable Bit	The Execute Disable bit allows memory to be marked as executable or non-executable, when combined with a supporting operating system. If code attempts to run in non-executable memory the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer overrun vulnerabilities and can thus help improve the overall security of the system. See the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* for more detailed information.
FLIT	Flow Control Unit. The Intel QPI Link layer's unit of transfer; 1 Flit = 80-bits.
Functional Operation	Refers to the normal operating conditions in which all processor specifications, including DC, system bus, signal quality, mechanical, and thermal, are satisfied.
GSSE	Extension of the SSE/SSE2 (Streaming SIMD Extensions) floating point instruction set to 256b operands.
HA	A Home Agent (HA) orders read and write requests to a piece of coherent memory.
ICU	Instruction Cache Unit. Part of the processor core architecture.
IFU	Instruction Fetch Unit. Part of the processor core.

continued...

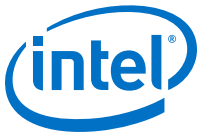


Term	Description
IIO	The Integrated I/O Controller. An I/O controller that is integrated in the processor die.
IMC	The Integrated Memory Controller. A Memory Controller that is integrated in the processor die.
IQ	Instruction Queue. Part of the core architecture.
Intel® ME	Intel® Management Engine
Intel® QuickData Technology	Intel® QuickData Technology is a platform solution designed to maximize the throughput of server data traffic across a broader range of configurations and server environments to achieve faster, scalable, and more reliable I/O.
Intel® QuickPath Interconnect (Intel® QPI)	A cache-coherent, link-based Interconnect specification for Intel processors, chipsets, and I/O bridge components.
Intel® 64 Technology	64-bit memory extensions to the IA-32 architecture. Further details on Intel 64 architecture and programming model can be found at http://developer.intel.com/technology/intel64/.
Intel® Turbo Boost Technology	A feature that opportunistically enables the processor to run a faster frequency. This results in increased performance of both single and multi-threaded applications.
Intel® TXT	Intel® Trusted Execution Technology
Intel® Virtualization Technology (Intel® VT)	Processor Virtualization which when used in conjunction with Virtual Machine Monitor software enables multiple, robust independent software environments inside a single platform.
Intel® VT-d	Intel® Virtualization Technology (Intel® VT) for Directed I/O. Intel VT-d is a hardware assist, under system software (Virtual Machine Manager or OS) control, for enabling I/O device Virtualization. Intel VT-d also brings robust security by providing protection from errant DMAs by using DMA remapping, a key feature of Intel VT-d.
Integrated Heat Spreader (IHS)	A component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface.
IOV	I/O Virtualization
IVR	Integrated Voltage Regulation (IVR): The processor supports several integrated voltage regulators.
Jitter	Any timing variation of a transition edge or edges from the defined Unit Interval (UI).
LGA 2011-3 Socket	The 2011-3 land FC-LGA package mates with the system board through this surface mount, 2011-3 contact socket.
LLC	Last Level Cache
LRDIMM	Load Reduced Dual In-line Memory Module
LRU	Least Recently Used. A term used in conjunction with cache allocation policy.
MESIF	Modified/Exclusive/Shared/Invalid/Forwarded. States used in conjunction with cache coherency
MLC	Mid Level Cache
NCTF	Non-Critical to Function: NCTF locations are typically redundant ground or non-critical reserved, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality.

continued...

Term	Description
NID	Node ID (NID) or NodeID (NID). The processor implements up to 4-bits of NodeID (NID).
NodeID	Node ID (NID) or NodeID (NID).
pcode	Pcode is microcode which is run on the dedicated microcontroller within the PCU.
PCH	Platform Controller Hub. A chipset with centralized platform capabilities including the main I/O interfaces along with display connectivity, audio features, power management, manageability, security and storage features.
PCU	Power Control Unit.
PCI Express 3.0	The third generation PCI Express specification that operates at twice the speed of PCI Express 2.0 (8 Gb/s); PCI Express 3.0 is completely backward compatible with PCI Express 1.0 and 2.0.
PCI Express 2.0	PCI Express Generation 2.0
PECI	Platform Environment Control Interface
Phit	An Intel® QPI terminology defining bits at physical layer.
Processor	Includes the 64-bit cores, uncore, I/Os and package
Processor Core	The term "processor core" refers to Si die itself which can contain multiple execution cores. Each execution core has an instruction cache, data cache, and 256-KB L2 cache. All execution cores share the L3 cache.
R3QPI	Intel QPI Agent. An internal logic block providing interface between internal Ring and external Intel QPI.
Rank	A unit of DRAM corresponding four to eight devices in parallel, ignoring ECC. These devices are usually, but not always, mounted on a single side of a DDR4 DIMM.
RDIMM	Registered Dual In-line Memory Module
RTID	Request Transaction IDs are credits issued by the Cbo to track outstanding transaction, and the RTIDs allocated to a Cbo are topology dependent.
SCI	System Control Interrupt. Used in ACPI protocol.
SKU	Stock Keeping Unit (SKU) is a subset of a processor type with specific features, electrical, power and thermal specifications. Not all features are supported on all SKUs. A SKU is based on specific use condition assumption.
SSE	Intel® Streaming SIMD Extensions (Intel® SSE)
SMBus	System Management Bus. A two-wire interface through which simple system and power management related devices can communicate with the rest of the system.
Storage Conditions	A non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor landings should not be connected to any supply voltages, have any I/Os biased or receive any clocks. Upon exposure to "free air" (that is, unsealed packaging or a device removed from packaging material) the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.
TAC	Thermal Averaging Constant
TDP	Thermal Design Power

continued...



Term	Description
TSOD	Temperature Sensor On DIMM
UDIMM	Unbuffered Dual In-line Memory Module
Uncore	The portion of the processor comprising the shared LLC cache, Cbo, IMC, HA, PCU, Ubox, IIO and Intel QPI link interface.
Unit Interval	Signaling convention that is binary and unidirectional. In this binary signaling, one bit is sent for every edge of the forwarded clock, whether it be a rising edge or a falling edge. If a number of edges are collected at instances t_1, t_2, t_n,...., t_k then the UI at instance "n" is defined as: $UI_n = t_n - t_{n-1}$
V_{CCIN}	Primary voltage input to the voltage regulators integrated into the processor.
VSS	Processor ground
V_{CCIO_IN}	IO voltage supply input
V_{CCD}	DDR power rail
x1	Refers to a Link or Port with one Physical Lane
x4	Refers to a Link or Port with four Physical Lanes
x8	Refers to a Link or Port with eight Physical Lanes
x16	Refers to a Link or Port with sixteen Physical Lanes

1.1.4 State of Data

The data contained within this document is final. It is the most accurate information available by the publication date of this document. Electrical DC specifications are based on estimated I/O buffer behavior.

2.0 Electrical Specifications

This chapter describes processor signaling, DC specifications, and signal quality. References to various interfaces (memory, PCIe*, Intel QPI, PECI, etc.) are also described.

2.1 Integrated Voltage Regulation

A new feature to the processor is the integration of platform voltage regulators into the processor. Due to this integration, the processor has one main voltage rail (V_{CCIN}) and a voltage rail for the memory interface (V_{CCD01}, V_{CCD23} - one for each memory channel pair), compared to five voltage rails (V_{CC}, V_{TTA}, V_{TTD}, V_{SA}, and V_{CCPLL}) on previous processors. The V_{CCIN} voltage rail will supply the integrated voltage regulators which in turn will regulate to the appropriate voltages for the cores, cache, and system agents. This integration allows the processor to better control on-die voltages to optimize for both performance and power savings. The processor V_{CCIN} rail will remain a sVID -based voltage with a loadline similar to the core voltage rail (called V_{CC}) in previous processors.

2.2 Processor Signaling

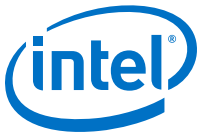
The Intel® Xeon® Processor E5-1600, E5-2600, and E5-4600 v3 Product Families include 2011 lands, which utilize various signaling technologies. Signals are grouped by electrical characteristics and buffer type into various signal groups. These include DDR4 (Reference Clock, Command, Control, and Data), PCI Express*, DMI2, Intel® QuickPath Interconnect, Platform Environmental Control Interface (PECI), System Reference Clock, SMBus, JTAG and Test Access Port (TAP), SVID Interface, Processor Asynchronous Sideband, Miscellaneous, and Power/Other signals. Refer to Table 7 on page 23 for details.

2.2.1 System Memory Interface Signal Groups

The system memory interface utilizes DDR4 technology, which consists of numerous signal groups. These include: Reference Clocks, Command Signals, Control Signals, and Data Signals. Each group consists of numerous signals, which may utilize various signaling technologies. Please refer to Table 7 on page 23 for further details. Throughout this chapter the system memory interface may be referred to as DDR4.

2.2.2 PCI Express Signals

The PCI Express Signal Group consists of PCI Express* ports 1, 2, and 3, and PCI Express miscellaneous signals. Please refer to Table 7 on page 23 for further details.



2.2.3 DMI2/PCI Express Signals

The Direct Media Interface Gen 2 (DMI2) sends and receives packets and/or commands to the PCH. The DMI2 is an extension of the standard PCI Express Specification. The DMI2/PCI Express Signals consist of DMI2 receive and transmit input/output signals and a control signal to select DMI2 or PCIe* 2.0 operation for port 0. Please refer to Table 7 on page 23 for further details.

2.2.4 Intel® QuickPath Interconnect (Intel® QPI)

The processor provides two Intel QPI ports for high speed serial transfer between other processors. Each port consists of two uni-directional links (for transmit and receive). A differential signaling scheme is utilized, which consists of opposite-polarity (DP, DN) signal pairs.

2.2.5 Platform Environmental Control Interface (PECI)

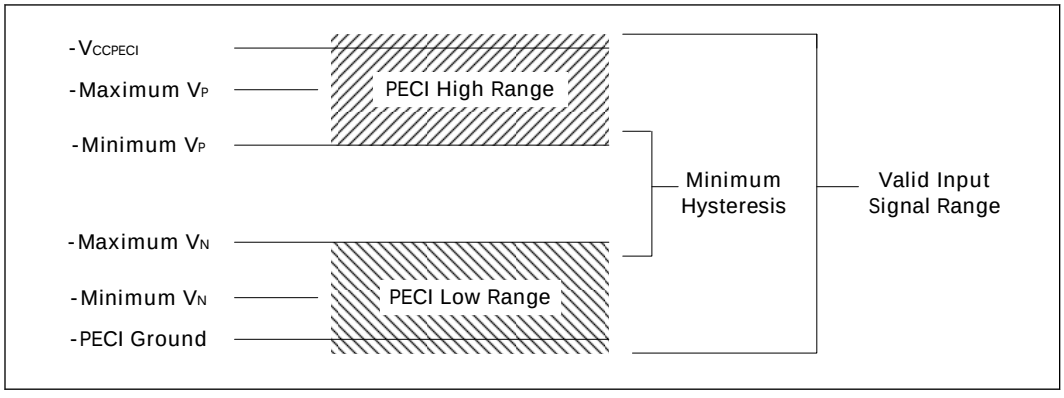
PECI is an Intel proprietary interface that provides a communication channel between Intel processors and chipset components to external system management logic and thermal monitoring devices. The processor contains a Digital Thermal Sensor (DTS) that reports a relative die temperature as an offset from Thermal Control Circuit (TCC) activation temperature. Temperature sensors located throughout the die are implemented as analog-to-digital converters calibrated at the factory. PECI provides an interface for external devices to read processor temperature, perform processor manageability functions, and manage processor interface tuning and diagnostics.

The PECI interface operates at a nominal voltage set by V_{CCPECI}. The set of DC electrical specifications shown in PECI DC Specifications on page 38 is used with devices normally operating from a V_{CCPECI} interface supply.

Input Device Hysteresis

The PECI client and host input buffers must use a Schmitt-triggered input design for improved noise immunity. Please refer to the following image and PECI DC Specifications on page 38.

Figure 1. Input Device Hysteresis



2.2.6 System Reference Clocks (BCLK{0/1}_DP, BCLK{0/1}_DN)

The processor Core, processor Uncore, Intel® QuickPath Interconnect link, PCI Express* and DDR4 memory interface frequencies) are generated from BCLK{0/1}_DP and BCLK{0/1}_DN signals. There is no direct link between core frequency and Intel QuickPath Interconnect link frequency (e.g., no core frequency to Intel QuickPath Interconnect multiplier). The processor maximum core frequency, Intel QuickPath Interconnect link frequency and DDR memory frequency are set during manufacturing. It is possible to override the processor core frequency setting using software (see the *Intel® 64 and IA-32 Architectures Software Developer's Manuals*). This permits operation at lower core frequencies than the factory set maximum core frequency.

The processor core frequency is configured during reset by using values stored within the device during manufacturing. The stored value sets the lowest core multiplier at which the particular processor can operate. If higher speeds are desired, the appropriate ratio can be configured via the IA32_PERF_CTL MSR (MSR 199h); Bits [15:0]. For details of operation at core frequencies lower than the maximum rated processor speed, refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* .

Clock multiplying within the processor is provided by the internal phase locked loop (PLL), which requires a constant frequency BCLK{0/1}_DP, BCLK{0/1}_DN input, with exceptions for spread spectrum clocking. DC specifications for the BCLK{0/1}_DP, BCLK{0/1}_DN inputs are provided in Processor Asynchronous Sideband DC Specifications on page 42. These specifications must be met while also meeting the associated signal quality specifications outlined in Signal Quality on page 45.

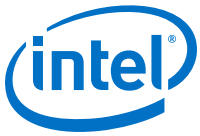
2.2.7 JTAG and Test Access Port (TAP) Signals

Due to the voltage levels supported by other components in the JTAG and Test Access Port (TAP) logic, Intel recommends the processor be first in the TAP chain, followed by any other components within the system. Please refer to the *Intel®Xeon® Processor E5-1600 and E5-2600 v3 Product Family Boundary Scan Description Language (BSDL)* file more details. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting an input of the appropriate voltage. Two copies of each signal may be required with each driving a different voltage level.

2.2.8 Processor Sideband Signals

The Intel® Xeon® processor E5-1600 and E5-2600 v3 product families includes asynchronous sideband signals that provide asynchronous input, output or I/O signals between the processor and the platform or Platform Controller Hub. Details can be found in Table 7 on page 23.

All Processor Asynchronous Sideband input signals are required to be asserted/de-asserted for a defined number of BCLKs in order for the processor to recognize the proper signal state, these are outlined in Processor Asynchronous Sideband DC Specifications on page 42 (DC specifications). Refer to Signal Quality on page 45 for applicable signal integrity specifications.



2.2.9 Power, Ground and Sense Signals

Processors also include various other signals, including power / ground and sense points. Details can be found in Table 7 on page 23.

Power and Ground Lands

All V_{CCD}, V_{CCIN}, and V_{CCIO_IN}, and V_{CCPECI} lands must be connected to their respective processor power planes, while all V_{SS} lands must be connected to the system ground plane.

For clean on-chip power distribution, processors include lands for all required voltage supplies. These are listed in the following table.

Table 3. Power and Ground Lands

Power and Ground Lands	Number of Lands	Comments
V_{CCIN}	173	Each V_{CCIN} land must be supplied with the voltage determined by the SVID Bus signals. Table 5 on page 21 defines the voltage level associated with each core SVID pattern. Table 15 on page 34 and Figure 4 on page 35 represent V_{CCIN} static and transient limits.
V_{CCD_01} V_{CCD_23}	56	Each V_{CCD} land is connected to a switchable 1.20 V supply, provide power to the processor DDR4 interface. V_{CCD} is also controlled by the SVID Bus. V_{CCD} is the generic term for V_{CCD_01} and V_{CCD_23}.
V_{CCIO_IN}	1	IO voltage supply input
V_{CCPECI}	1	Power supply for PECI.
V_{SS}	631	Ground

Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the Intel® Xeon® processor E5-1600 and E5-2600 v3 product families is capable of generating large current swings between low and full power states. This may cause voltages on power planes to sag below their minimum values if bulk decoupling is not adequate. Large electrolytic bulk capacitors (CBULK), help maintain the output voltage during current transients, for example coming out of an idle condition. Care must be taken in the baseboard design to ensure that the voltages provided to the processor remain within the specifications listed in Table 13 on page 31. Failure to do so can result in timing violations or reduced lifetime of the processor.

Voltage Identification (VID)

The reference voltage or the VID setting is set via the SVID communication bus between the processor and the voltage regulator controller chip. The VID settings are the nominal voltages to be delivered to the processor's V_{CCIN} lands. Table 5 on page 21 specifies the reference voltage level corresponding to the VID value transmitted over serial VID. The VID codes will change due to temperature and/or current load changes in order to minimize the power and to maximize the performance of the part. The specifications are set so that a voltage regulator can operate with all supported frequencies.

Individual processor VID values may be calibrated during manufacturing such that two processor units with the same core frequency may have different default VID settings.

The processor uses voltage identification signals to support automatic selection of V_{CCIN} power supply voltage. If the processor socket is empty (SKTOCC_N high), or a "not supported" response is received from the SVID bus, then the voltage regulation circuit cannot supply the voltage that is requested, the voltage regulator must disable itself or not power on. Vout MAX register (30h) is programmed by the processor to set the maximum supported VID code and if the programmed VID code is higher than the VID supported by the VR, then VR will respond with a "not supported" acknowledgment.

SVID Commands

The processor provides the ability to operate while transitioning to a new VID setting and its associated processor voltage rail (V_{CCIN}). This is represented by a DC shift. It should be noted that a low-to-high or high-to-low voltage state change may result in as many VID transitions as necessary to reach the target voltage. Transitions above the maximum specified VID are not supported. The processor supports the following VR commands:

- SetVID_Fast (20 mV/µs)
- SetVID_Slow (5 mV/µs)
- Slew Rate Decay (downward voltage only and it's a function of the output capacitance's time constant) commands. Table 5 on page 21 includes SVID step sizes and DC shift ranges. Minimum and maximum voltages must be maintained as shown in Table 13 on page 31.

The VRM or EVRD utilized must be capable of regulating its output to the value defined by the new VID.

Power source characteristics must be guaranteed to be stable whenever the supply to the voltage regulator is stable.

SetVID Fast Command

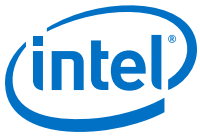
The SetVID_Fast command contains the target VID in the payload byte. The range of voltage is defined in the VID table. The VR should ramp to the new VID setting with a fast slew rate as defined in the slew rate data register. It is minimum of 20 mV/µs, depending on the amount of decoupling capacitance.

The SetVID_Fast command is preemptive. The VR interrupts its current processes and moves to the new VID. The SetVID_Fast command operates on 1 VR address at a time. This command is used in the processor for package C6 fast exit.

SetVID Slow

The SetVID_Slow command contains the target VID in the payload byte. The range of voltage is defined in the VID table. The VR should ramp to the new VID setting with a "slow" slew rate as defined in the slow slew rate data register. The SetVID_Slow is nominally 4x slower than the SetVID_Fast slew rate.

The SetVID_Slow command is preemptive, the VR interrupts its current processes and moves to the new VID. This is the instruction used for normal P-state voltage change. This command is used in the processor for the Intel Enhanced SpeedStep Technology transitions.



SetVID Decay

The SetVID_Decay command is the slowest of the DVID transitions. It is normally used for VID down transitions. The VR does not control the slew rate, the output voltage declines with the output load current only.

The SetVID_Decay command is preemptive, the VR interrupts its current processes and moves to the new VID. This command is used in the processor for package C6 entry, allowing capacitor discharge by the leakage, thus saving energy.This command is normally used in VID down direction in the processor package C6 entry.

SVID Power State Functions: SetPS

The processor has three power state functions and these will be set seamlessly via the SVID bus using the SetPS command. Based on the power state command, the SetPS commands sends information to VR controller to configure the VR to improve efficiency, especially at light loads. For example, typical power states are:

- PS0(00h): Represents full power or active mode
- PS1(01h): Represents a light load 5A to 20A
- PS2(02h): Represents a very light load <5A

Note: In PS2 some CPUs can have idle or leakage currents up to 20A. the MBVR must handle high idle currents if they are present even in PS2 condition.

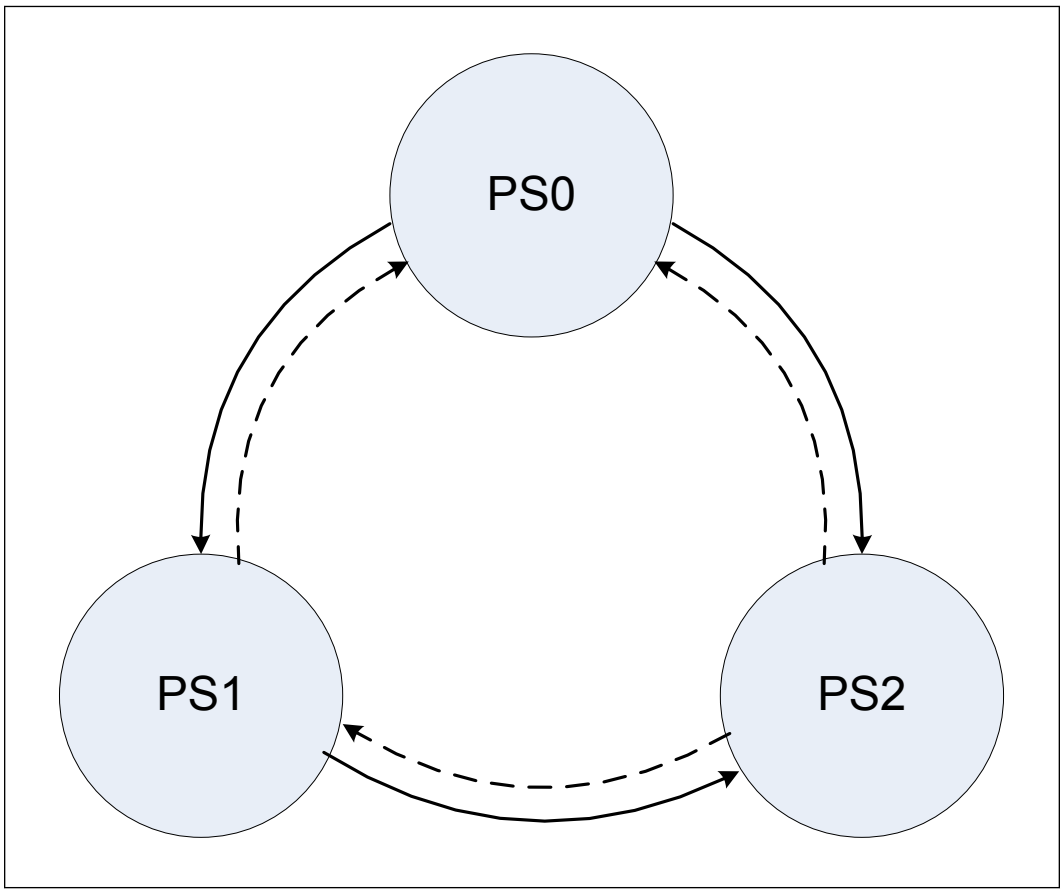
The VR may change its configuration to meet the processor's power needs with greater efficiency. For example, it may reduce the number of active phases, transition from CCM (Continuous Conduction Mode) to DCM (Discontinuous Conduction Mode) mode, reduce the switching frequency or pulse skip, or change to asynchronous regulation. For example, typical power states are 00h = run in normal mode; a command of 01h = shed phases mode, and an 02h = pulse skip.

The VR may reduce the number of active phases from PS(00h) to PS(01h) or PS(00h) to PS(02h) for example. There are multiple VR design schemes that can be used to maintain a greater efficiency in these different power states, please work with your VR controller suppliers for optimizations.

If a power state is not supported by the controller, the slave should acknowledge the SetPS command and enter the lowest power state that is supported.

If the VR is in a low power state and receives a SetVID command moving the VID up then the VR exits the low power state to normal mode (PS0) to move the voltage up as fast as possible. The processor must re-issue low power state (PS1 or PS2) command if it is in a low current condition at the new higher voltage. See the figure below for VR power state transitions.

Figure 2. VR Power State Transitions



SVID Voltage Rail Addressing

The processor addresses 3 different voltage rail control segments within VR12.5 (V_{CCIN}, V_{CCD_01}, and V_{CCD_23}). The SVID data packet contains a 4-bit addressing code:

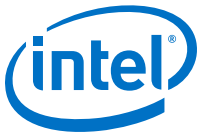
Table 4. SVID Address Usage

PWM Address (HEX)	Intel® Xeon® Processor E5-1600 and E5-2600 v3 Product Families
00	V_{CCIN}
01	NA
02	V_{CCD_01}
03	+1 not used
04	V_{CCD_23}
05	+1 not used

Note:

1. Check with VR vendors for determining the physical address assignment method for their controllers.
2. VR addressing is assigned on a per voltage rail basis.
3. Dual VR controllers will have two addresses with the lowest order address, always being the higher phase count.

continued...



PWM Address (HEX)	Intel® Xeon® Processor E5-1600 and E5-2600 v3 Product Families
4. For future platform flexibility, the VR controller should include an address offset, as shown with +1 not used.	

Table 5. VR12.5 Reference Code Voltage Identification (VID) Table

HEX	VCCIN	HEX	VCCIN	HEX	VCCIN	HEX	VCCIN	HEX	VCCIN	HEX	VCCIN
00	0.00	55	1.34	78	1.69	9B	2.04	BE	2.39	E1	2.74
33	1.00	56	1.35	79	1.70	9C	2.05	BF	2.40	E2	2.75
34	1.01	57	1.36	7A	1.71	9D	2.06	C0	2.41	E3	2.76
35	1.02	58	1.37	7B	1.72	9E	2.07	C1	2.42	E4	2.77
36	1.03	59	1.38	7C	1.73	9F	2.08	C2	2.43	E5	2.78
37	1.04	5A	1.39	7D	1.74	A0	2.09	C3	2.44	E6	2.79
38	1.05	5B	1.40	7E	1.75	A1	2.10	C4	2.45	E7	2.80
39	1.06	5C	1.41	7F	1.76	A2	2.11	C5	2.46	E8	2.81
3A	1.07	5D	1.42	80	1.77	A3	2.12	C6	2.47	E9	2.82
3B	1.08	5E	1.43	81	1.78	A4	2.13	C7	2.48	EA	2.83
3C	1.09	5F	1.44	82	1.79	A5	2.14	C8	2.49	EB	2.84
3D	1.10	60	1.45	83	1.80	A6	2.15	C9	2.50	EC	2.85
3E	1.11	61	1.46	84	1.81	A7	2.16	CA	2.51	ED	2.86
3F	1.12	62	1.47	85	1.82	A8	2.17	CB	2.52	EE	2.87
40	1.13	63	1.48	86	1.83	A9	2.18	CC	2.53	EF	2.88
41	1.14	64	1.49	87	1.84	AA	2.19	CD	2.54	F0	2.89
42	1.15	65	1.50	88	1.85	AB	2.20	CE	2.55	F1	2.90
43	1.16	66	1.51	89	1.86	AC	2.21	CF	2.56	F2	2.91
44	1.17	67	1.52	8A	1.87	AD	2.22	D0	2.57	F3	2.92
45	1.18	68	1.53	8B	1.88	AE	2.23	D1	2.58	F4	2.93
46	1.19	69	1.54	8C	1.89	AF	2.24	D2	2.59	F5	2.94
47	1.20	6A	1.55	8D	1.90	B0	2.25	D3	2.60	F6	2.95
48	1.21	6B	1.56	8E	1.91	B1	2.26	D4	2.61	F7	2.96
49	1.22	6C	1.57	8F	1.92	B2	2.27	D5	2.62	F8	2.97
4A	1.23	6D	1.58	90	1.93	B3	2.28	D6	2.63	F9	2.98
4B	1.24	6E	1.59	91	1.94	B4	2.29	D7	2.64	FA	2.99
4C	1.25	6F	1.60	92	1.95	B5	2.30	D8	2.65	FB	3.00
4D	1.26	70	1.61	93	1.96	B6	2.31	D9	2.66	FC	3.01
4E	1.27	71	1.62	94	1.97	B7	2.32	DA	2.67	FD	3.02
4F	1.28	72	1.63	95	1.98	B8	2.33	DB	2.68	FE	3.03
50	1.29	73	1.64	96	1.99	B9	2.34	DC	2.69	FF	3.04
51	1.30	74	1.65	97	2.00	BA	2.35	DD	2.70		

continued...

HEX	VCCIN	HEX	VCCIN	HEX	VCCIN	HEX	VCCIN	HEX	VCCIN	HEX	VCCIN
52	1.31	75	1.66	98	2.01	BB	2.36	DE	2.71		
53	1.320	76	1.67	99	2.02	BC	2.37	DF	2.72		
54	1.33	77	1.68	9A	2.03	BD	2.38	E0	2.73		

Note:
1. 00h = Off State
2. VID Range HEX 01-32 are not used by the Intel® Xeon® processor E5-1600 and E5-2600 v3 product families
3. For VID Ranges supported see Table 13 on page 31
4. V_{CCD} is a fixed voltage of 1.20V

Reserved or Unused Signals

All Reserved (RSVD) signals must not be connected. Connection of these signals to V_{CCIN}, V_{CCD}, V_{SS}, or to any other signal (including each other) can result in component malfunction or incompatibility with future processors.

For reliable operation, always connect unused inputs or bi-directional signals to an appropriate signal level. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs maybe left unconnected; however, this may interfere with some Test Access Port (TAP) functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bi-directional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability. Resistor values should be within ± 20% of the impedance of the baseboard trace.

2.2.10 Reserved or Unused Signals

All Reserved (RSVD) signals must not be connected. Connection of these signals to V_{CCIN}, V_{CCD}, V_{SS}, or to any other signal (including each other) can result in component malfunction or incompatibility with future processors.

For reliable operation, always connect unused inputs or bi-directional signals to an appropriate signal level. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs maybe left unconnected; however, this may interfere with some Test Access Port (TAP) functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bi-directional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability. Resistor values should be within ± 20% of the impedance of the baseboard trace.

2.3 Signal Group Summary

Signals are grouped by buffer type and similar characteristics as listed in the following table. The buffer type indicates which signaling technology and specifications apply to the signals.

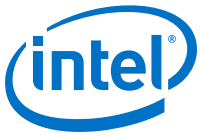


Table 6. Signal Description Buffer Types

Signal	Description
Analog	Analog reference or output. May be used as a threshold voltage or for buffer compensation
Asynchronous[1]	Signal has no timing relationship with any system reference clock.
CMOS	CMOS buffers: 1.05V
DDR4	buffers: 1.2V
DMI2	Direct Media Interface Gen 2 signals. These signals are compatible with PCI Express* 2.0 and 1.0 Signaling Environment AC Specifications.
Intel® QPI	Current-mode 9.6 GT/s, 8.0 GT/s, and 6.4 GT/s, forwarded-clock Intel QuickPath Interconnect signaling
Open Drain CMOS	Open Drain CMOS (ODCMOS) buffers: 1.05V tolerant
PCI Express*	PCI Express* interface signals. These signals are compatible with PCI Express 3.0 Signaling Environment AC Specifications and are AC coupled. The buffers are not 3.3-V tolerant. Refer to the PCIe specification.
Reference	Voltage reference signal.
SSTL	Source Series Terminated Logic (JEDEC SSTL_15)

Note:
1. Qualifier for a buffer type.

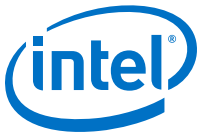
Table 7. Signal Groups

Differential/Single Ended	Buffer Type	Signal
DDR4 Reference Clocks		
Differential	SSTL Output	DDR{0/1/2/3}_CLK_D[N/P][3:0]
DDR4 Command Signals		
Single-ended	SSTL Output	DDR{0/1/2/3}_ACT_N DDR{0/1/2/3}_BA[1:0] DDR{0/1/2/3}_BG[1:0] DDR{0/1/2/3}_MA[17] DDR{0/1/2/3}_MA[16]/_RAS_N DDR{0/1/2/3}_MA[15]/_CAS_N DDR{0/1/2/3}_MA[14]/_WE_N DDR{0/1/2/3}_MA[13:0] DDR{0/1/2/3}_PAR
DDR4 Control Signals		
Single-ended	SSTL Output	DDR{0/1/2/3}_CS_N[9:8] DDR{0/1/2/3}CS_N[7]/CID[4] DDR{0/1/2/3}CS_N[6]/CID[3] DDR{0/1/2/3}_CS_N[5:4] DDR{0/1/2/3}CS_N[3]/CID[1] DDR{0/1/2/3}CS_N[2]/CID[0] DDR{0/1/2/3}_CS_N[1:0] DDR{0/1/2/3}_CID[2] DDR{0/1/2/3}_ODT[5:0] DDR{0/1/2/3}_CKE[5:0]

continued...

Differential/Single Ended	Buffer Type	Signal
DDR4 Data Signals		
Differential	SSTL Input/Output	DDR{0/1/2/3}_DQS_D[N/P][17:0]
Single ended	SSTL Input/Output	DDR{0/1/2/3}_DQ[63:0] DDR{0/1/2/3}_ECC[7:0]
DDR4 Miscellaneous Signals		
Single ended	SSTL Input	DDR{0/1/2/3}_ALERT_N
	CMOS Input *Note:* Input voltage from platform cannot exceed 1.08V max.	DRAM_PWR_OK_C01 DRAM_PWR_OK_C23
	CMOS 1.2V Output	DDR_RESET_C{01/23}_N
	Open Drain CMOS Input/Output	DDR_SCL_C01 DDR_SCL_C23 DDR_SDA_C01 DDR_SDA_C23
	DC Output	DDR01_VREF DDR23_VREF
PCI Express* Port 1, 2, & 3 Signals		
Differential	PCI Express* Input	PE1A_RX_D[N/P][3:0] PE1B_RX_D[N/P][7:4] PE2A_RX_D[N/P][3:0] PE2B_RX_D[N/P][7:4] PE2C_RX_D[N/P][11:8] PE2D_RX_D[N/P][15:12] PE3A_RX_D[N/P][3:0] PE3B_RX_D[N/P][7:4] PE3C_RX_D[N/P][11:8] PE3D_RX_D[N/P][15:12]
Differential	PCI Express* Output	PE1A_TX_D[N/P][3:0] PE1B_TX_D[N/P][7:4] PE2A_TX_D[N/P][3:0] PE2B_TX_D[N/P][7:4] PE2C_TX_D[N/P][11:8] PE2D_TX_D[N/P][15:12] PE3A_TX_D[N/P][3:0] PE3B_TX_D[N/P][7:4] PE3C_TX_D[N/P][11:8] PE3D_TX_D[N/P][15:12]
PCI Express* Miscellaneous Signals		
Single ended	Open Drain CMOS Input/Output	PE_HP_SCL
		PE_HP_SDA
DMI2/PCI Express* Signals		
Differential	DMI2 Input	DMI_RX_D[N/P][3:0]
	DMI2 Output	DMI_TX_D[N/P][3:0]
Intel® QuickPath Interconnect (Intel® QPI) Signals		

continued...



Differential/Single Ended	Buffer Type	Signal
Differential	Intel® QPI Input	QPI{0/1}_DRX_D[N/P][19:0] QPI{0/1}_CLKRX_D[N/P]
	Intel® QPI Output	QPI{0/1}_DTX_D[N/P][19:0] QPI{0/1}_CLKTX_D[N/P]
Platform Environmental Control Interface (PECI)		
Single ended	PECI Input/Output	PECI
System Reference Clock (BCLK{0/1})		
Differential	CMOS 1.05V Input	BCLK{0/1}_D[N/P]
JTAG & TAP Signals		
Single ended	CMOS 1.05V Input	TCK TDI TMS TRST_N
	CMOS 1.05V Input/Output	PREQ_N
	CMOS1.05V Output	PRDY_N
	Open Drain CMOS Input/Output	BPM_N[7:0]
	Open Drain CMOS Output	TDO
Serial VID Interface (SVID) Signals		
Single ended	CMOS 1.05V Input	SVIDALERT_N
	Open Drain CMOS Input/Output	SVIDDATA
	Open Drain CMOS Output	SVIDCLK
Processor Asynchronous Sideband Signals		
Single ended	CMOS 1.05V Input	BIST_ENABLE BMCINIT DEBUG_EN_N FRMAGENT PWRGOOD PMSYNC RESET_N SAFE_MODE_BOOT SOCKET_ID[1:0] TXT_AGENT TXT_PLTEN
	CMOS 1.05V Output	FIVR_FAULT
	Open Drain CMOS Input/Output	CATERR_N MEM_HOT_C01_N MEM_HOT_C23_N MSMI_N PM_FAST_WAKE_N PROCHOT_N
	Open Drain CMOS Output	ERROR_N[2:0] THERMTRIP_N
Miscellaneous Signals		

continued...

Differential/Single Ended	Buffer Type	Signal
	CMOS 1.05V Input	EAR_N
	Output	SKTOCC_N
Power/Other Signals		
	Power / Ground	V_{CCIN}, V_{CCD_01}, V_{CCD_23}, V_{CCIO_IN}, V_{CCPECI}, V_{SS}
	Sense Points	VCCIN_SENSE VSS_VCCIN_SENSE

Note:
1. Refer to "Signal Descriptions" for signal description details.
2. DDR{0/1/2/3} refers to DDR4 Channel 0, DDR4 Channel 1, DDR4 Channel 2 and DDR4 Channel 3.

Table 8. Signals with On-Die Weak PU/PD

Signal Name	Pull Up/Pull Down	Rail	Value	Units
BIST_ENABLE	Pull Up	VCCIO_IN	5K-15K	Ω
BMCINIT	Pull Down	VSS	5K-15K	Ω
DEBUG_EN_N	Pull Up	VCCIO_IN	5K-15K	Ω
EAR_N	Pull Up	VCCIO_IN	5K-15K	Ω
FRMAGENT	Pull Down	VSS	5K-15K	Ω
PM_FAST_WAKE_N	Pull Up	VCCIO_IN	5K-15K	Ω
PREQ_N	Pull Up	VCCIO_IN	5K-15K	Ω
SAFE_MODE_BOOT	Pull Down	VSS	5K-15K	Ω
SOCKET_ID[1:0]	Pull Down	VSS	5K-15K	Ω
TCK	Pull Down	VSS	5K-15K	Ω
TDI	Pull Up	VCCIO_IN	5K-15K	Ω
TMS	Pull Up	VCCIO_IN	5K-15K	Ω
TRST_N	Pull Up	VCCIO_IN	5K-15K	Ω
TXT_AGENT	Pull Down	VSS	5K-15K	Ω
TXT_PLTEN	Pull Up	VCCIO_IN	5K-15K	Ω

2.4 Power-On Configuration (POC) Options

Several configuration options can be configured by hardware. The processor samples its hardware configuration at reset, on the active-to-inactive transition of RESET_N, or upon assertion of PWRGOOD (inactive-to-active transition). For specifics on these options, please refer to the table below.

The sampled information configures the processor for subsequent operation. These configuration options cannot be changed except by another reset transition of the latching signal (RESET_N or PWRGOOD).

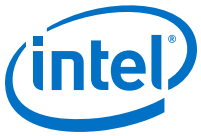


Table 9. Power-On Configuration Option Lands

Configuration Option	Land Name	Notes
Output tri state	PROCHOT_N	1
Execute BIST (Built-In Self Test)	BIST_ENABLE	2
Enable Service Processor Boot Mode	BMCINIT	3
Power-up Sequence Halt	EAR_N	3
Enable Intel® Trusted Execution Technology (Intel® TXT) Platform	TXT_PLTEN	3
Enable Bootable Firmware Agent	FRMAGENT	3
Enable Intel Trusted Execution Technology (Intel TXT) Agent	TXT_AGENT	3
Enable Safe Mode Boot	SAFE_MODE_BOOT	3
Configure Socket ID	SOCKET_ID[1:0]	3
Enables debug from cold boot	DEBUG_EN_N	3

Note:

1. Output tri-state option enables Fault Resilient Booting (FRB), for FRB details see the Fault Resilient Booting (FRB) Section. The signal used to latch PROCHOT_N for enabling FRB mode is RESET_N.
2. BIST_ENABLE is sampled at RESET_N de-assertion
3. This signal is sampled after PWRGOOD assertion.

2.5 Fault Resilient Booting (FRB)

The Intel® Xeon® processor v3 product families supports both socket and core level Fault Resilient Booting (FRB), which provides the ability to boot the system as long as there is one processor functional in the system. One limitation to socket level FRB is that the system cannot boot if the legacy socket that connects to an active PCH becomes unavailable since this is the path to the system BIOS. See the table below for a list of output tri-state FRB signals.

Socket level FRB will tri-state processor outputs via the PROCHOT_N signal. Assertion of the PROCHOT_N signal through RESET_N de-assertion will tri-state processor outputs. Note, that individual core disabling is also supported for those cases where disabling the entire package is not desired.

The Intel® Xeon® processor v3 product families extends the FRB capability to the core granularity by maintaining a register in the Uncore so that BIOS or another entity can disable one or more specific processor cores.

Table 10. Fault Resilient Booting (Output Tri-State) Signals

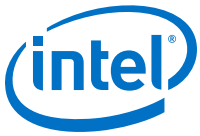
Output Tri-State Signal Groups	Signals
Intel QPI	QPI0_CLKTX_DN[1:0] QPI0_CLKTX_DP[1:0] QPI0_DTX_DN[19:00] QPI0_DTX_DP[19:00] QPI1_CLKTX_DN[1:0] QPI1_CLKTX_DP[1:0] QPI1_DTX_DN[19:00]

continued...

Output Tri-State Signal Groups	Signals
	QPI1_DTX_DP[19:00]
PCI Express*	PE1A_TX_DN[3:0] PE1A_TX_DP[3:0] PE1B_TX_DN[7:4] PE1B_TX_DP[7:4] PE2A_TX_DN[3:0] PE2A_TX_DP[3:0] PE2B_TX_DN[7:4] PE2B_TX_DP[7:4] PE2C_TX_DN[11:8] PE2C_TX_DP[11:8] PE2D_TX_DN[15:12] PE2D_TX_DP[15:12] PE3A_TX_DN[3:0] PE3A_TX_DP[3:0] PE3B_TX_DN[7:4] PE3B_TX_DP[7:4] PE3C_TX_DN[11:8] PE3C_TX_DP[11:8] PE3D_TX_DN[15:12] PE3D_TX_DP[15:12] PE_HP_SCL PE_HP_SDA
DMI2	DMI_TX_DN[3:0] DMI_TX_DP[3:0]
SMBus	DDR_SCL_C01 DDR_SDA_C01 DDR_SCL_C23 DDR_SDA_C23
Processor Sideband	CATERR_N ERROR_N[2:0] BPM_N[7:0] PRDY_N THERMTRIP_N PROCHOT_N PECI MEM_HOT_C01_N MEM_HOT_C23_N PM_FAST_WAKE_N FIVR_FAULT
SVID	SVIDCLK SVIDDATA

2.6 Mixing Processors

Intel supports and validates two configurations only in which all processors operate with the same Intel® QuickPath Interconnect frequency, core frequency, power segment, and have the same internal cache sizes. Mixing components operating at different internal clock frequencies is not supported and will not be validated by Intel. Combining processors from different power segments is also not supported.



Note: All processors within a system must run at a common maximum non-Turbo ratio. The system BIOS may be required to program the FLEX_RATIO register if mixed frequency processors are populated.

Not all operating systems can support dual processors with mixed frequencies. Mixing processors of different steppings but the same model (as per CPUID instruction) is supported, provided there is no more than one stepping delta between the processors, for example, S and S+1.

S and S+1 is defined as mixing of two CPU steppings in the same platform where one CPU is S (stepping) = CPUID.(EAX=01h):EAX[3:0], and the other is S+1 = CPUID.(EAX=01h):EAX[3:0]+1. The stepping ID is found in EAX[3:0] after executing the CPUID instruction with Function 01h. Details regarding the CPUID instruction are provided in the *Intel® 64 and IA-32 Architectures Software Developer's Manuals*, *Volume 2A: Instruction Set Reference, A-M*.

2.7 Flexible Motherboard Guidelines (FMB)

The Flexible Motherboard (FMB) guidelines are estimates of the maximum values the Intel® Xeon® processor v3 product families will have over certain time periods. The values are only estimates and actual specifications for future processors may differ. Processors may or may not have specifications equal to the FMB value in the foreseeable future. System designers should meet the FMB values to ensure their systems will be compatible with future processors.

2.8 Absolute Maximum and Minimum Ratings

The table below specifies absolute maximum and minimum ratings. At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

Although the processor contains protective circuitry to resist damage from Electro-Static Discharge (ESD), precautions should always be taken to avoid high static voltages or electric fields.

Table 11. Processor Absolute Minimum and Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{CCIN}	Processor input voltage with respect to Vss	-0.3	1.98	V
V_{CCD}	Processor IO supply voltage for DDR4 (standard voltage) with respect to V_{SS}	-0.3	1.35	V
V_{CCIO_IN}	IO voltage supply input with respect to V_{SS}	-0.3	1.35	V
V_{CCPECI}	Power supply for PECI with respect to V_{SS}	-0.3	1.35	V
Note: 1. For functional operation, all processor electrical, signal quality, mechanical, and thermal specifications must be satisfied.				

continued...

Symbol	Parameter	Min	Max	Unit
2. Overshoot and undershoot voltage guidelines for input, output, and I/O signals are outlined in Overshoot/ Undershoot Tolerance on page 46. Excessive Overshoot or undershoot on any signal will likely result in permanent damage to the processor.				

Storage Conditions Specifications

Environmental storage condition limits define the temperature and relative humidity limits to which the device is exposed to while being stored in a Moisture Barrier Bag. The specified storage conditions are for component level prior to board attach (see notes in the table below for post board attach limits).

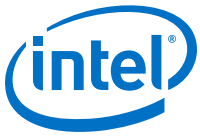
The table below specifies absolute maximum and minimum storage temperature limits which represent the maximum or minimum device condition beyond which damage, latent or otherwise, may occur. The table also specifies sustained storage temperature, relative humidity, and time-duration limits. These limits specify the maximum or minimum device storage conditions for a sustained period of time. At conditions outside sustained limits, but within absolute maximum and minimum ratings, quality and reliability may be affected.

Table 12. Storage Condition Ratings

Symbol	Parameter	Min	Max	Unit
$T_{absolute\ storage}$	The minimum/maximum device storage temperature beyond which damage (latent or otherwise) may occur when subjected to for any length of time.	-25	125	°C
$T_{sustained\ storage}$	The minimum/maximum device storage temperature for a sustained period of time.	-5	40	°C
$T_{short\ term\ storage}$	The ambient storage temperature (in shipping media) for a short period of time.	-20	85	°C
$RH_{sustained\ storage}$	The maximum device storage relative humidity for a sustained period of time.	60% @ 24		°C
$Time_{sustained\ storage}$	A prolonged or extended period of time; typically associated with sustained storage conditions Unopened bag, includes 6 months storage time by customer.	0	30	months
$Time_{short\ term\ storage}$	A short period of time (in shipping media).	0	72	hours

Note:

1. Storage conditions are applicable to storage environments only. In this scenario, the processor must not receive a clock, and no lands can be connected to a voltage bias. Storage within these limits will not affect the long-term reliability of the device. For functional operation, please refer to the processor case temperature specifications.
2. These ratings apply to the Intel component and do not include the tray or packaging.
3. Failure to adhere to this specification can affect the long-term reliability of the processor.
4. Non-operating storage limits post board attach: Storage condition limits for the component once attached to the application board are not specified. Intel does not conduct component level certification assessments post board attach given the multitude of attach methods, socket types and board types used by customers. Provided as general guidance only, Intel board products are specified and certified to meet the following temperature and humidity limits (Non-Operating Temperature Limit: -40C to 70C & Humidity: 50% to 90%, non condensing with a maximum wet bulb of 28°C).
5. Device storage temperature qualification methods follow JEDEC High and Low Temperature Storage Life Standards: *JESD22-A119* (low temperature) and *JESD22-A103* (high temperature).



2.9 DC Specifications

DC specifications are defined at the processor pads, unless otherwise noted. DC specifications are only valid while meeting specifications for case temperature (TCASE specified in the *Intel® Xeon® Processor E5-1600 and E5-2600 v3 Product Families Thermal/Mechanical Specification and Design Guide (TMSDG)*), clock frequency, and input voltages. Care should be taken to read all notes associated with each specification.

2.9.1 Voltage and Current Specifications

Table 13. Voltage Specification

Symbols	Parameter	Voltage Plane	Min	Nom	Max	Unit	Notes[1]
V_{CCIN}	Input to Integrated Voltage Regulator (Launch - FMB)	V_{CCIN}	1.47	1.82	1.85	V	2, 3, 4, 5, 8, 10, 13
V_{VID_STEP} (V_{CCIN}, V_{CCD})	VID step size during a transition			10.0		mV	6
V_{CCD} (V_{CCD_01}, V_{CCD_23})	I/O Voltage for DDR4 (Standard Voltage)	V_{CCD}	0.97*V_{CCD_NOM}	1.2	1.044*V_{CCD_NOM}	V	7, 9, 10, 11, 12

Note:

1. Unless otherwise noted, all specifications in this table apply to all processors. These specifications are based on final characterization.
2. These voltages are targets only. A variable voltage source should exist on systems in the event that a different voltage is required.
3. The V_{CCIN} voltage specification requirements are measured across the remote sense pin pairs (V_{CCIN_SENSE} and $V_{SS\_VCCIN\_SENSE}$) on the processor package. Voltage measurement should be taken with a DC to 100 MHz bandwidth oscilloscope limit (or DC to 20MHz for older model oscilloscopes), using a 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of the ground wire on the probe should be less than 5 mm to ensure external noise from the system is not coupled in the scope probe.
4. Refer to Table 15 on page 34 and corresponding Figure 4 on page 35. The processor should not be subjected to any static V_{CCIN} level that exceeds the V_{CCIN_MAX} associated with any particular current. Failure to adhere to this specification can shorten processor lifetime.
5. Minimum V_{CCIN} and maximum I_{CCIN} are specified at the maximum processor case temperature (T_{CASE}) shown in the *Intel® Xeon® Processor E5-1600 and E5-2600 v3 Product Families Thermal/Mechanical Specification and Design Guide (TMSDG)*. I_{CCIN_MAX} is specified at the relative V_{CC_MAX} point on the V_{CCIN} load line. The processor is capable of drawing I_{CCIN_MAX} for up to 4 ms.
6. This specification represents the V_{CCIN} reduction or V_{CCIN} increase due to each VID transition. For Voltage Identification (VID) see Voltage Identification (VID) on page 17. AC timing requirements for VID transitions are included in Figure 3 on page 32.
7. Baseboard bandwidth is limited to 20 MHz.
8. FMB is the flexible motherboard guidelines. See Flexible Motherboard Guidelines (FMB) on page 29 for details.
9. DC + AC + Ripple = Total Tolerance
10. For SVID Power State Functions (SetPS) see SVID Power State Functions: SetPS on page 19.
11. V_{CCD} tolerance at processor pins. Required in order to meet +/-5% tolerance at processor die.
12. The V_{CCD01}, V_{CCD23} voltage specification requirements are measured across vias on the platform. Choose V_{CCD01} or V_{CCD23} vias close to the socket and measure with a DC to 100MHz bandwidth oscilloscope limit (or DC to 20 MHz for older model oscilloscopes), using 1.5 pF maximum probe capacitance, and 1M ohm minimum impedance. The maximum length of the ground wire on the probe should be less than 5 mm to ensure external noise from the system is not coupled in the scope probe.
13. V_{CCIN} has a V_{boot} setting of 0.0V and is not included in the PWRGOOD indication.
14. Nominal voltage for future processor drop-in compatibility is 0.95V.

Figure 3. Serial VID Interface (SVID) Signals Clock Timings

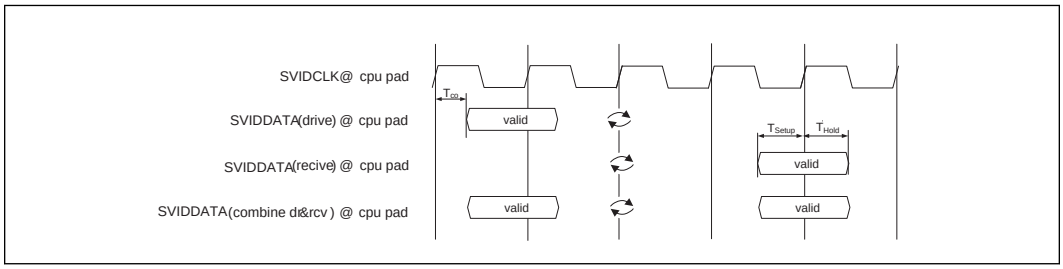
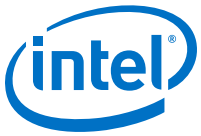


Table 14. CPU Power Rails Load Specification

Segment	TDP	ICCIN_MAX @ VCCIN(A)	ICC_ MAX @ VCCIO_ IN (A)	ICC_ MAX @ VCCPECI (A)	ICCD01_ MAX (A)[5]	ICCD23_ MAX (A)[5]	ICCIN_ TDC[3] @ VCCIN(A)	ICC_ TDC[3] @ VCCIO_ IN(A)	ICC_ TDC[3] @ VCCPECI(A)	ICCD01_ TDC (A)[5]	ICCD23_ TDC[3] (A)[5]	Pmax[4] @ VCCIN(W)	Pmax_ Package[4] (W)	Notes[1]
Segment Optimized	145W 18-Core	176	0.1	0.001	1.4 (2.45)	1.4 (2.45)	83	0.02	0.001	0.8 (2.2)	0.8 (2.2)	288	290	2, 4
	135W 16-Core	162	0.1	0.001	1.4 (2.45)	1.4 (2.45)	76	0.02	0.001	0.8 (2.2)	0.8 (2.2)	267	270	2, 4
	120W 145W 14-Core	176	0.1	0.001	1.4 (2.45)	1.4 (2.45)	83	0.02	0.001	0.8 (2.2)	0.8 (2.2)	288	290	2, 4
	120W 14-Core	142	0.1	0.001	1.4 (2.45)	1.4 (2.45)	68	0.02	0.001	0.8 (2.2)	0.8 (2.2)	237	240	2, 4
Workstation	160W 10-Core	189	0.1	0.001	1.4 (2.45)	1.4 (2.45)	92	0.02	0.001	0.8 (2.2)	0.8 (2.2)	307	320	2, 4
	140W 8-Core	170	0.1	0.001	1.4 (2.45)	1.4 (2.45)	80	0.02	0.001	0.8 (2.2)	0.8 (2.2)	279	280	2,4
	140W 6-Core	170	0.1	0.001	1.4 (2.45)	1.4 (2.45)	80	0.02	0.001	0.8 (2.2)	0.8 (2.2)	279	280	2,4
	140W 4-Core	170	0.1	0.001	1.4 (2.45)	1.4 (2.45)	80	0.02	0.001	0.8 (2.2)	0.8 (2.2)	279	280	2,4
Frequency Optimized	135W 8-Core	162	0.1	0.001	1.4 (2.45)	1.4 (2.45)	76	0.02	0.001	0.8 (2.2)	0.8 (2.2)	267	270	2, 4
	135W 6-Core	162	0.1	0.001	1.4 (2.45)	1.4 (2.45)	76	0.02	0.001	0.8 (2.2)	0.8 (2.2)	267	270	2, 4
	135W 4-Core	162	0.1	0.001	1.4 (2.45)	1.4 (2.45)	76	0.02	0.001	0.8 (2.2)	0.8 (2.2)	267	270	2, 4
	105W 4-Core	123	0.1	0.001	1.4 (2.45)	1.4 (2.45)	59	0.02	0.001	0.8 (2.2)	0.8 (2.2)	208	210	2, 4

continued...



Segment	TDP	I_{CCIN_MAX} @ V_{CCIN}(A)	I_{CC_MAX} @ V_{CCIO_IN} (A)	I_{CC_MAX} @ V_{CCPECI} (A)	I_{CCD01_MAX} (A)[5]	I_{CCD23_MAX} (A)[5]	I_{CCIN_TDC}[3] @ V_{CCIN}(A)	I_{CC_TDC}[3] @ V_{CCIO_IN}(A)	I_{CC_TDC}[3] @ V_{CCPECI}(A)	I_{CCD01_TDC} (A)[5]	I_{CCD23_TDC}[3] (A)[5]	P_{max}[4] @ V_{CCIN}(W)	$P_{max\_Package}$[4] (W)	Notes[1]
Advanced Server	135W 12-Core	162	0.1	0.001	1.4 (2.45)	1.4 (2.45)	76	0.02	0.001	0.8 (2.2)	0.8 (2.2)	267	270	2, 4
	120W 12-Core	142	0.1	0.001	1.4 (2.45)	1.4 (2.45)	68	0.02	0.001	0.8 (2.2)	0.8 (2.2)	237	240	2, 4
	105W 10-Core	123	0.1	0.001	1.4 (2.45)	1.4 (2.45)	59	0.02	0.001	0.8 (2.2)	0.8 (2.2)	208	210	2, 4
Standard Server	90W 8-Core	104	0.1	0.001	1.4 (2.45)	1.4 (2.45)	50	0.02	0.001	0.8 (2.2)	0.8 (2.2)	178	180	2, 4
	85W 8-Core	98	0.1	0.001	1.4 (2.45)	1.4 (2.45)	47	0.02	0.001	0.8 (2.2)	0.8 (2.2)	168	170	2, 4
	85W 6-Core	98	0.1	0.001	1.4 (2.45)	1.4 (2.45)	47	0.02	0.001	0.8 (2.2)	0.8 (2.2)	168	170	2,4
Basic	8-Core	98	0.1	0.001	1.4 (2.45)	1.4 (2.45)	47	0.02	0.001	0.8 (2.2)	0.8 (2.2)	168	170	2, 4
	85W 6-Core	98	0.1	0.001	1.4 (2.45)	1.4 (2.45)	47	0.02	0.001	0.8 (2.2)	0.8 (2.2)	168	170	2, 4
Low Power	65W 12-Core	73	0.1	0.001	1.4 (2.45)	1.4 (2.45)	35	0.02	0.001	0.8 (2.2)	0.8 (2.2)	127	130	2, 4
	55W 8-Core	61	0.1	0.001	1.4 (2.45)	1.4 (2.45)	30	0.02	0.001	0.8 (2.2)	0.8 (2.2)	107	210	2, 4
Embedded	120W 10-Core	142	0.1	0.001	1.4 (2.45)	1.4 (2.45)	68	0.02	0.001	0.8 (2.2)	0.8 (2.2)	237	240	2, 4
	105W 12-Core	123	0.1	0.001	1.4 (2.45)	1.4 (2.45)	59	0.02	0.001	0.8 (2.2)	0.8 (2.2)	208	210	2, 4
	85W 8-Core	98	0.1	0.001	1.4 (2.45)	1.4 (2.45)	47	0.02	0.001	0.8 (2.2)	0.8 (2.2)	168	170	2, 4
	75W 12-Core	86	0.1	0.001	1.4 (2.45)	1.4 (2.45)	41	0.02	0.001	0.8 (2.2)	0.8 (2.2)	149	150	2, 4
	75W 10-Core	86	0.1	0.001	1.4 (2.45)	1.4 (2.45)	41	0.02	0.001	0.8 (2.2)	0.8 (2.2)	149	150	2, 4
	75W 8-Core	86	0.1	0.001	1.4 (2.45)	1.4 (2.45)	41	0.02	0.001	0.8 (2.2)	0.8 (2.2)	149	150	2, 4
	52W 6-Core	58	0.1	0.001	1.4 (2.45)	1.4 (2.45)	28	0.02	0.001	0.8 (2.2)	0.8 (2.2)	102	104	2, 4
	50W 6-Core	56	0.1	0.001	1.4 (2.45)	1.4 (2.45)	27	0.02	0.001	0.8 (2.2)	0.8 (2.2)	99	100	2, 4

Note:

1. Unless otherwise noted, all specifications in this table apply to all processors. These specifications are based on final characterization.

Segment	TDP	ICCIN_MAX @ VCCIN(A)	ICC_ MAX @ VCCIO_ IN (A)	ICC_ MAX @ VCCPECI (A)	ICCD01_ MAX (A)[5]	ICCD23_ MAX (A)[5]	ICCIN_ TDC[3] @ VCCIN(A)	ICC_ TDC[3] @ VCCIO_ IN(A)	ICC_ TDC[3] @ VCCPECI(A)	ICCD01_ TDC (A)[5]	ICCD23_ TDC[3] (A)[5]	Pmax[4] @ VCCIN(W)	Pmax_ Package[4] (W)	Notes[1]

2. FMB is the flexible motherboard guidelines. See Flexible Motherboard Guidelines (FMB) on page 29 for further details.
3. I_{CCIN_TDC} (Thermal Design Current) is the sustained (DC equivalent) current that the processor is capable of drawing indefinitely and should be used for the voltage regulator thermal assessment. The voltage regulator is responsible for monitoring its temperature and asserting the necessary signal to inform the processor of a thermal excursion.
4. Minimum V_{CCIN} and maximum I_{CCIN} are specified at the maximum processor case temperature (T_{CASE}). I_{CCIN_MAX} is specified at the relative V_{CCIN_MAX} point on the V_{CCIN} load line. The processor is capable of drawing I_{CCIN_MAX} for up to 4 ms.
5. The numbers in parentheses are due to a memory initialization load pulse occurring at system boot that may last up to 5s.

Table 15. V_{CCIN} Static and Transient Tolerance

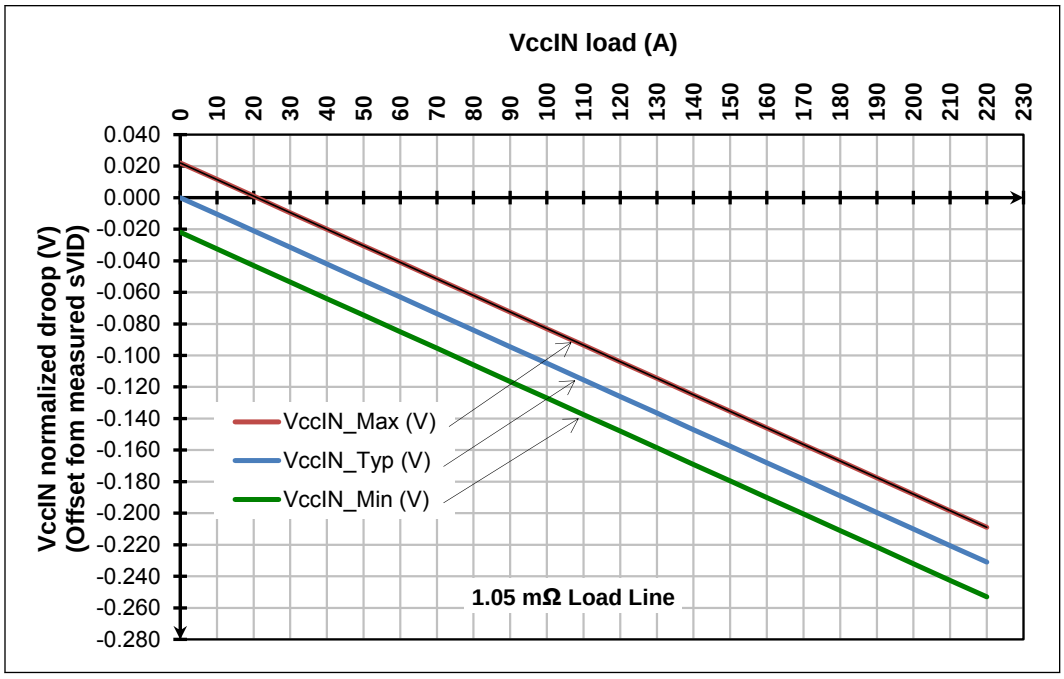
I_{CCIN} (A)	V_{CCIN_Max} (V)	V_{CCIN_Nom} (V)	V_{CCIN_Min} (V)	Notes
0	VID + 0.022	VID - 0.000	VID - 0.022	
10	VID + 0.012	VID - 0.011	VID - 0.033	
20	VID + 0.001	VID - 0.021	VID - 0.043	
30	VID - 0.010	VID - 0.032	VID - 0.054	
40	VID - 0.020	VID - 0.042	VID - 0.064	
50	VID - 0.031	VID - 0.053	VID - 0.075	
60	VID - 0.041	VID - 0.063	VID - 0.085	
70	VID - 0.052	VID - 0.074	VID - 0.096	
80	VID - 0.062	VID - 0.084	VID - 0.106	
90	VID - 0.073	VID - 0.095	VID - 0.117	
100	VID - 0.083	VID - 0.105	VID - 0.127	
110	VID - 0.094	VID - 0.116	VID - 0.138	
120	VID - 0.104	VID - 0.126	VID - 0.148	
130	VID - 0.115	VID - 0.137	VID - 0.159	
140	VID - 0.125	VID - 0.147	VID - 0.169	
150	VID - 0.136	VID - 0.158	VID - 0.180	
160	VID - 0.146	VID - 0.168	VID - 0.190	
170	VID - 0.157	VID - 0.179	VID - 0.201	
180	VID - 0.167	VID - 0.189	VID - 0.211	
190	VID - 0.178	VID - 0.200	VID - 0.222	
200	VID - 0.188	VID - 0.210	VID - 0.232	
210	VID - 0.199	VID - 0.221	VID - 0.243	
220	VID - 0.209	VID - 0.231	VID - 0.253	
Note:				

continued...

I_{CCIN} (A)	V_{CCIN_Max} (V)	V_{CCIN_Nom} (V)	V_{CCIN_Min} (V)	Notes

1. The V_{CCIN_MIN} and V_{CCIN_MAX} loadlines represent static and transient limits. Please see Die Voltage Validation on page 35 for V_{CCIN} Overshoot specifications.
2. This table is intended to aid in reading discrete points on graph in Figure 4 on page 35.
3. The loadlines specify voltage limits at the die measured at the V_{CCIN_SENSE} and $V_{SS\_VCCIN\_SENSE}$ lands. Voltage regulation feedback for voltage regulator circuits must also be taken from processor V_{CCIN_SENSE} and $V_{SS\_VCCIN\_SENSE}$ lands.
4. The Adaptive Loadline Positioning slope is 1.05 mΩ (mohm) with +/- 22mV TOB (Tolerance of Band).
5. Processor current (I_{CCIN}) ranges are valid up to I_{CCIN_MAX} of the processor SKU as defined in the previous table above.

Figure 4. V_{CCIN} Static and Transient Tolerance Loadlines



2.9.2 Die Voltage Validation

Overshoot events at the processor must meet the specifications in Table 16 on page 36 when measured across the V_{CCIN_SENSE} and $V_{SS\_VCCIN\_SENSE}$ lands. Overshoot events that are < 10 ns in duration may be ignored. These measurements of processor die level overshoot should be taken with a 100 MHz bandwidth limited oscilloscope.

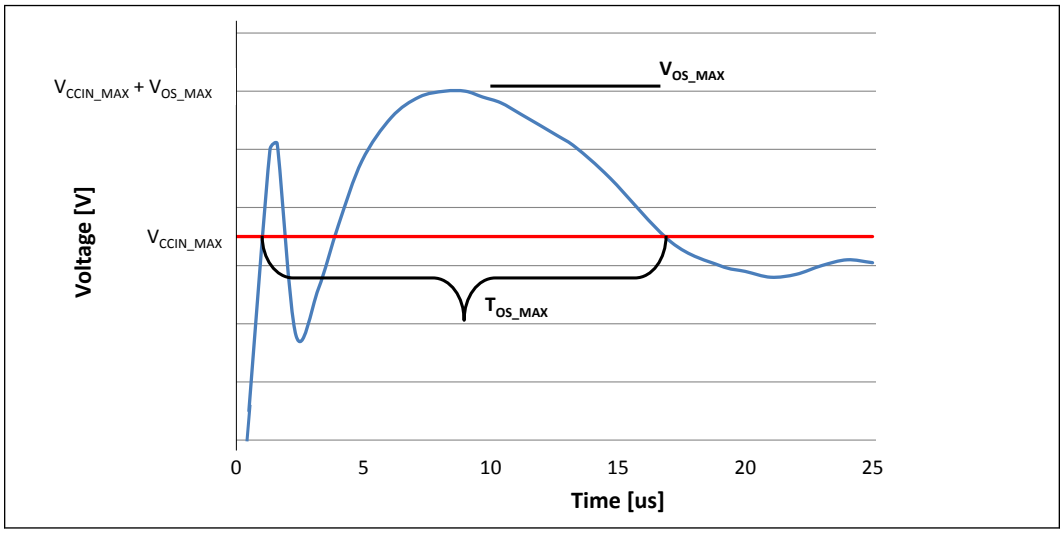
V_{CCIN} Overshoot Specifications

The Intel® Xeon® processor E5-1600 and E5-2600 v3 product families can tolerate short transient overshoot events where V_{CCIN} exceeds the VID voltage when transitioning from a high-to-low current load condition. This overshoot cannot exceed VID + V_{OS_MAX} (V_{OS_MAX} is the maximum allowable overshoot above VID). These specifications apply to the processor die voltage as measured across the V_{CCIN_SENSE} and $V_{SS\_VCCIN\_SENSE}$ lands.

Table 16. V_{CCIN} Overshoot Specifications

Symbol	Parameter	Min	Max	Units	Figure	Notes
V_{OS_MAX}	Magnitude of V_{CCIN} overshoot above VID		50	mV	Figure 5 on page 36	
T_{OS_MAX}	Time duration of V_{CCIN} overshoot above V_{CCIN_Max} value at the new lighter load		25	µs	Figure 5 on page 36	

Figure 5. V_{CCIN} Overshoot Example Waveform



Note:

1. V_{OS_MAX} is the measured overshoot voltage above V_{CCIN_MAX}.
2. T_{OS_MAX} is the measured time duration above V_{CCIN_MAX}.
3. V_{CCIN_MAX} = VID + TOB

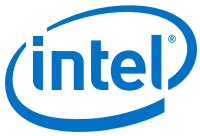
2.9.3 Signal DC Specifications

For additional specifications, refer to Related Publications on page 9.

2.9.3.1 DDR4 Signal DC Specifications

Symbol	Parameter	Min	Nom	Max	Units	Notes[1]
I_{IL}	Input Leakage Current	-1.4		+1.4	mA	9
Data Signals						
R_{ON}	DDR4 Data Buffer On Resistance	27		33	ohm	6
Data ODT	On-Die Termination for Data Signals	45		55	ohm	8
Reference Clock and Command Signals						
V_{OL}	Output Low Voltage		(V_{CCD} / 2)* (R_{ON} /		V	2, 7

continued...



Symbol	Parameter	Min	Nom	Max	Units	Notes[1]
			(R_{ON} + R_{VTT_TERM}))			
V_{OH}	Output High Voltage		V_{CCD} - ((V_{CCD} / 2)* (R_{ON} / (R_{ON} + R_{VTT_TERM})))		V	2, 5, 7
Data Signals						
V_{OL}	Output Low Voltage		Varies			10
V_{OH}	Output High Voltage		V_{CCD}			
Reference Clock Signal						
R_{ON}	DDR4 Clock Buffer On Resistance	27		33	ohm	6
Command Signals						
R_{ON}	DDR4 Command Buffer On Resistance	16		20	ohm	6
R_{ON}	DDR4 Reset Buffer On Resistance		78		ohm	6
$V_{OL\_CMOS1.2V}$	Output Low Voltage, Signals DDR_RESET_ C{01/23}_N			0.2*V_{CCD}	V	1, 2
$V_{OH\_CMOS1.2V}$	Output High Voltage, Signals DDR_RESET_ C{01/23}_N	0.9*V_{CCD}			V	1, 2
Control Signals						
R_{ON}	DDR4 Control Buffer On Resistance	27		33	ohm	6
DDR4 Miscellaneous Signals						
ALERT_N	On-Die Termination for Parity Error Signals	81	90	99	ohm	
V_{IL}	Input Low Voltage DRAM_PWR_OK_C{01/23}			304	mV	2, 3
V_{IH}	Input High Voltage DRAM_PWR_OK_C{01/23}	800			mV	2, 4, 5

Note:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The voltage rail V_{CCD} which will be set to 1.2V nominal depending on the voltage of all DIMMs connected to the processor.
3. V_{IL} is the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
4. V_{IH} is the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
5. V_{IH} and V_{OH} may experience excursions above V_{CCD}. However, input signal drivers must comply with the signal quality specifications. Refer to Signal Quality on page 45.
6. This is the pull down driver resistance. Reset drive does not have a termination.
7. R_{VTT_TERM} is the termination on the DIMM and not controlled by the processor. Refer to the applicable DIMM datasheet.
8. The minimum and maximum values for these signals are programmable by BIOS to one of the pairs.
9. Input leakage current is specified for all DDR4 signals.
10. Vol = Ron * [VCCD/(Ron + Rtt_Eff)], where Rtt_Eff is the effective pull-up resistance of all DIMMs in the system, including ODTs and series resistors on the DIMMs.

2.9.3.2 PECI DC Specifications

Symbol	Definition and Conditions	Min	Max	Units	Figure	Notes[1]
V_{In}	Input Voltage Range	-0.150	V_{CCPECI} + 0.150	V		
$V_{Hysteresis}$	Hysteresis	0.100 * V_{CCPECI}		V		
V_N	Negative-edge threshold voltage	0.275 * V_{CCPECI}	0.500 * V_{CCPECI}	V	Figure 1 on page 15	2
V_P	Positive-edge threshold voltage	0.550 * V_{CCPECI}	0.725 * V_{CCPECI}	V	Figure 1 on page 15	2
I_{Source}	Pullup Resistance (V_{OH} = 0.75 * V_{CCPECI})	-6.00		mA		
I_{Leak+}	High impedance state leakage to V_{CCIO_IN} (V_{leak} = V_{OL})	50	200	µA		
R_{ON}	High impedance leakage to GND (V_{leak} = V_{OH})	20	36	Ω		
C_{Bus}	Bus capacitance per node	N/A	10	pF		4, 5
V_{Noise}	Signal noise immunity above 300 MHz	0.100 * V_{CCPECI}	N/A	V_{p-p}		
	Output Edge Rate (50 ohm to V_{SS}, between V_{IL} and V_{IH})	1.5	4	V/ns		

Note:

1. V_{CCPECI} supplies the PECI interface. PECI behavior does not affect V_{CCPECI} min/max specification.
2. It is expected that the PECI driver will take into account, the variance in the receiver input thresholds and consequently, be able to drive its output within safe limits (-0.150 V to 0.275*V_{CCPECI} for the low level and 0.725*V_{CCPEC} to V_{CCPECI}+0.150 V for the high level).
3. The leakage specification applies to powered devices on the PECI bus.
4. One node is counted for each client and one node for the system host. Extended trace lengths might appear as additional nodes.
5. Excessive capacitive loading on the PECI line may slow down the signal rise/fall times and consequently limit the maximum bit rate at which the interface can operate.

2.9.3.3 System Reference Clock (BCLK{0/1}) DC Specifications

Symbol	Parameter	Signal	Min	Max	Unit	Figure	Notes[1]
$V_{BCLK\_diff\_ih}$	Differential Input High Voltage	Differential	0.150	N/A	V	Figure 6 on page 39	9
$V_{BCLK\_diff\_il}$	Differential Input Low Voltage	Differential		-0.150	V	Figure 6 on page 39	9
V_{cross} (abs)	Absolute Crossing Point	Single Ended	0.250	0.550	V	Figure 7 on page 40 Figure 8 on page 40	2, 4, 7, 9

continued...

Symbol	Parameter	Signal	Min	Max	Unit	Figure	Notes[1]
V_{cross} (rel)	Relative Crossing Point	Single Ended	0.250 + 0.5*(VH $_{avg}$ - 0.700)	0.550 + 0.5*(VH $_{avg}$ - 0.700)	V	Figure 7 on page 40	3, 4, 5, 9
ΔV_{cross}	Range of Crossing Points	Single Ended	N/A	0.140	V	Figure 9 on page 40	6, 9
V_{TH}	Threshold Voltage	Single Ended	Vcross - 0.1	Vcross + 0.1	V		9
I_{IL}	Input Leakage Current	N/A		1.50	mA		8, 9
C_{pad}	Pad Capacitance	N/A	1.12	1.7	pF		9

Note:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Crossing Voltage is defined as the instantaneous voltage value when the rising edge of BCLK{0/1}_DN is equal to the falling edge of BCLK{0/1}_DP.
3. V_{Havg} is the statistical average of the VH measured by the oscilloscope.
4. The crossing point must meet the absolute and relative crossing point specifications simultaneously.
5. V_{Havg} can be measured directly using "Vtop" on Agilent* and "High" on Tektronix oscilloscopes.
6. V_{CROSS} is defined as the total variation of all crossing voltages as defined in Note 3.
7. The rising edge of BCLK{0/1}_DN is equal to the falling edge of BCLK{0/1}_DP.
8. For Vin between 0 and Vih.
9. Specifications can be validated at the pin.

Figure 6. BCLK{0/1} Differential Clock Measurement Point for Ringback

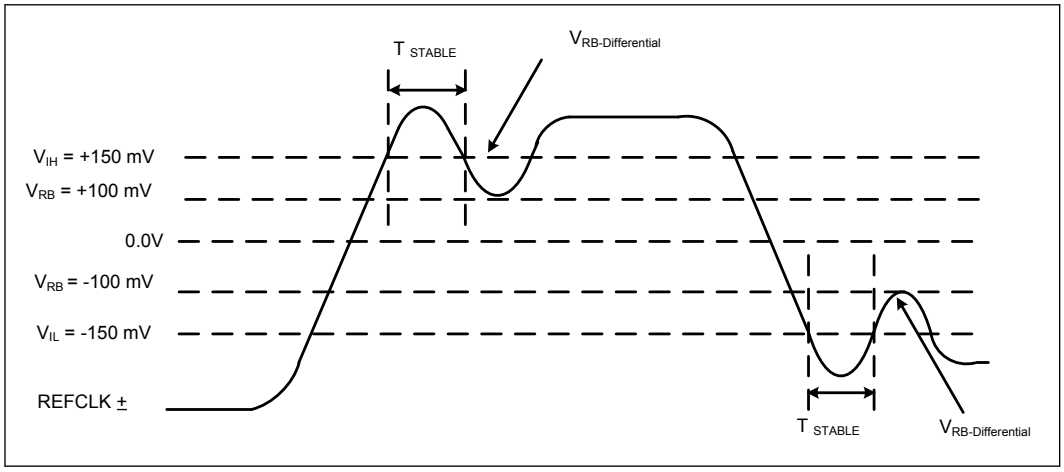


Figure 7. BCLK{0/1} Differential Clock Crosspoint Specification

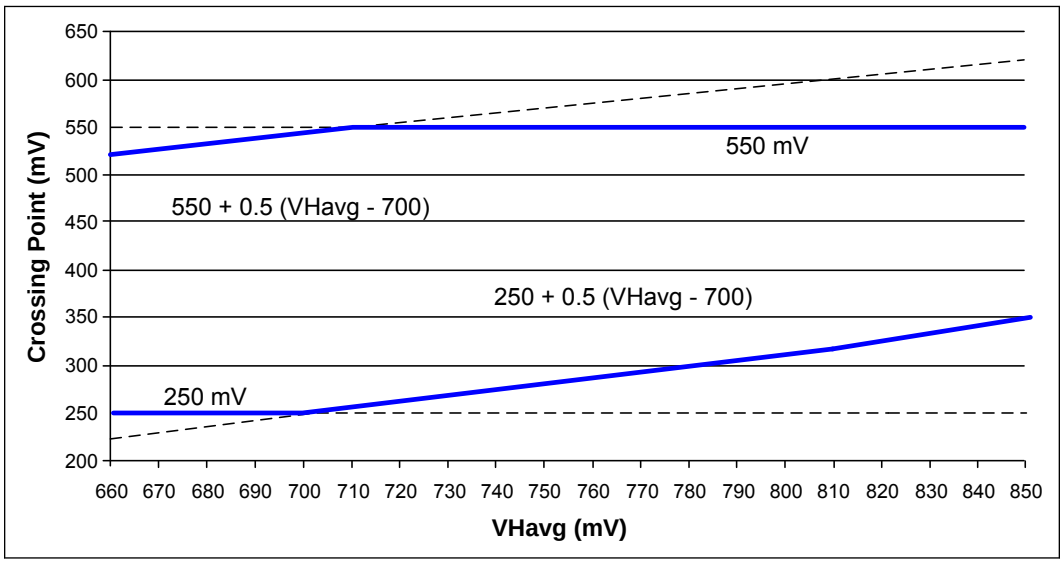


Figure 8. BCLK{0/1} Single Ended Clock Measurement Points for Absolute Cross Point and Swing

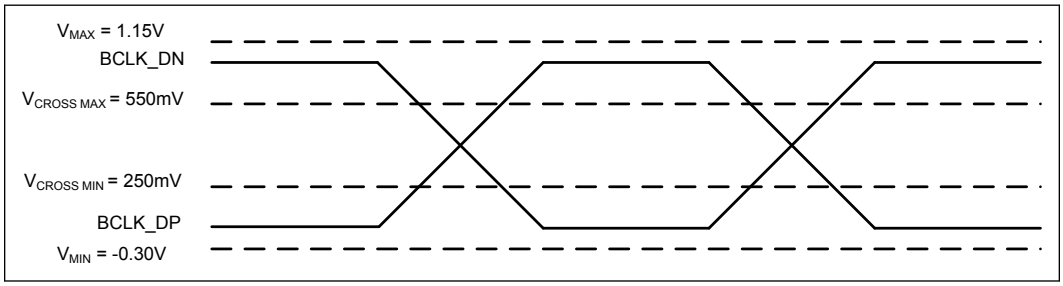
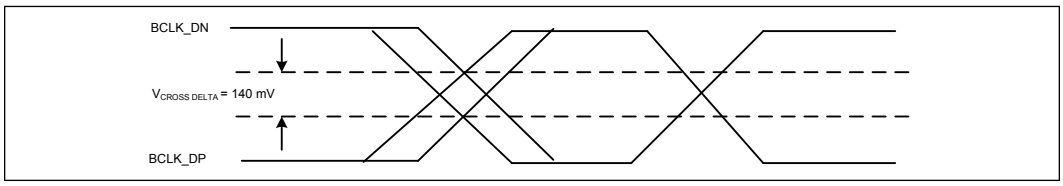


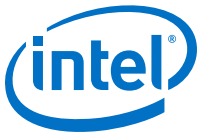
Figure 9. BCLK{0/1} Single Ended Clock Measure Points for Delta Cross Point



2.9.3.4 SMBus DC Specifications

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage		0.3*V_{CCIO_IN}	V	
V_{IH}	Input High Voltage	0.7*V_{CCIO_IN}		V	
$V_{Hysteresis}$	Hysteresis	0.1*V_{CCIO_IN}		V	
V_{OL}	Output Low Voltage		0.2*V_{CCIO_IN}	V	
R_{ON}	Buffer On Resistance	4	14	Ω	

continued...



Symbol	Parameter	Min	Max	Units	Notes
I_L	Leakage Current Signals	50	200	µA	
	Output Edge Rate (50 ohm to V_{CCIO_IN}, between V_{IL} and V_{IH})	0.05	0.6	V/ns	1

Note:
1. Value obtained through test bench with 50Ω pull up to V_{CCIO_IN}.

2.9.3.5 JTAG and TAP Signals DC Specifications

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage		0.4*V_{CCIO_IN}	V	
V_{IH}	Input High Voltage	0.8*V_{CCIO_IN}		V	
V_{IL}	Input Low Voltage: TCK		0.4*V_{CCIO_IN}	V	
V_{IH}	Input High Voltage: TCK	0.6*V_{CCIO_IN}		V	
V_{OL}	Output Low Voltage		0.2*V_{CCIO_IN}	V	
$V_{Hysteresis}$	Hysteresis	0.1*V_{CCIO_IN}			
R_{ON}	Buffer On Resistance Signals BPM_N[7:0], TDO	4	14	Ω	
I_{IL}	Input Leakage Current Signals	50	200	µA	
	Output Edge Rate (50 ohm to V_{CCIO_IN}) Signal: BPM_N[7:0], PRDY_N, TDO	0.2	1.5	V/ns	1

Note:
1. These are measured between V_{IL} and V_{IH}.
2. The signal edge rate must be met or the signal must transition monotonically to the asserted state.

2.9.3.6 Serial VID Interface (SVID) DC Specifications

Symbol	Parameter	Min	Nom	Max	Units	Notes
V_{IL}	Input Low Voltage Signals SVIDDATA, SVIDALERT_N			0.4*V_{CCIO_IN}	V	1
V_{IH}	Input High Voltage Signals SVIDDATA, SVIDALERT_N	0.7*V_{CCIO_IN}			V	1
V_{OL}	Output Low Voltage Signals: SVIDCLK, SVIDDATA			0.2*V_{CCIO_IN}	V	1, 5
$V_{Hysteresis}$	Hysteresis	0.05*V_{CCIO_IN}			V	1
R_{ON}	Buffer On Resistance Signals SVIDCLK, SVIDDATA	4		14	Ω	2
I_{IL}	Input Leakage Current	50		200	µA	3
	Input Edge Rate Signal: SVIDALERT_N	0.05			V/ns	4
	Output Edge Rate	0.20		1.5	V/ns	4, 5

Note:
1. V_{CCIO_IN} refers to instantaneous V_{CCIO_IN}.
2. Measured at 0.31*V_{CCIO_IN}.
3. Vin between 0V and V_{CCIO_IN} (applies to SVIDDATA and SVIDALERT_N only).
4. These are measured between V_{IL} and V_{IH}.
5. Value obtained through test bench with 50Ω pull up to V_{CCIO_IN}.

2.9.3.7 Processor Asynchronous Sideband DC Specifications

Symbol	Parameter	Min	Max	Units	Notes
CMOS1.05v Signals					
$V_{IL\_CMOS1.05V}$	Input Low Voltage		0.4*V_{CCIO_IN}	V	1, 2
$V_{IH\_CMOS1.05V}$	Input High Voltage	0.6*V_{CCIO_IN}		V	1, 2
$I_{IL\_CMOS1.05V}$	Input Leakage Current	50	200	µA	1,2
Open Drain CMOS (ODCMOS) Signals					
V_{IL_ODCMOS}	Input Low Voltage Signals: CATERR_N, MSMI_N, PM_FAST_WAKE_N		0.4*V_{CCIO_IN}	V	1, 2
V_{IL_ODCMOS}	Input Low Voltage Signals: MEM_HOT_C01/23_N, PROCHOT_N		0.3*V_{CCIO_IN}	V	1, 2
V_{IH_ODCMOS}	Input High Voltage	0.7*V_{CCIO_IN}		V	1, 2
V_{OL_ODCMOS}	Output Low Voltage		0.2*V_{CCIO_IN}	V	1, 2
$V_{Hysteresis}$	Hysteresis Signals: MEM_HOT_C01/23_N, PROCHOT_N	0.1*V_{CCIO_IN}			
$V_{Hysteresis}$	Hysteresis Signal: CATERR_N, MSMI_N, PM_FAST_WAKE_N	0.05*V_{CCIO_IN}			
I_L	Input Leakage Current	50	200	µA	
R_{ON}	Buffer On Resistance	4	14	Ω	1, 2
	Output Edge Rate Signal: MEM_HOT_C{01/23}_ N, ERROR_N[2:0], THERMTRIP, PROCHOT_N	0.05	0.60	V/ns	3
	Output Edge Rate Signal: CATERR_N, MSMI_N, PM_FAST_WAKE_N	0.2	1.5	V/ns	3

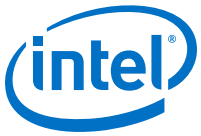
Note:
1. This table applies to the processor sideband and miscellaneous signals specified in Table 7 on page 23.
2. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
3. These are measured between V_{IL} and V_{IH}.

2.9.3.8 Miscellaneous Signals DC Specifications

Symbol	Parameter	Min	Nominal	Max	Units
SKTOCC_N Signal					
$V_{O\_ABS\_MAX}$	Output Absolute Max Voltage		3.30	3.50	V
I_{OMAX}	Output Max Current			1	mA

2.10 Package C-State Power Specifications

The following table lists the processor package C-state power specifications for the various processor SKUs.

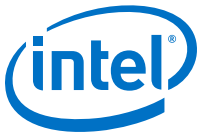


Segment	Model Number	TDP	C1E (W) [2]	C3 (W) [2]	C6 (W)
Segment Optimized	E5-2699 v3	145W 18-Core	56	36	14
	E5-2698 v3	135W 16-Core	47	33	14
	E5-2697 v3	145W 14-Core	45	34	14
	E5-2695 v3	120W 14-Core	46	34	14
	E5-2683 v3	120W 14-Core	55	38	20
Workstation	E5-2687 v3	160W 10-Core	41	31	13
	E5-1680 v3	140W 8-Core	34	25	12
	E5-1660 v3	140W 8-Core	34	25	12
	E5-1650 v3	140W 6-Core	30	22	12
	E5-1630 v3	140W 4-Core	26	20	12
	E5-1620 v3	140W 4-Core	26	20	12
Frequency Optimized	E5-2667 v3	135W 8-Core	32	26	12
	E5-2643 v3	135W 6-Core	32	26	12
	E5-2637 v3	135W 4-Core	30	25	12
	E5-2623 v3	105W 4-Core	33	26	12
Advanced Server	E5-2690 v3	135W 12-Core	38	30	13
	E5-2680 v3	120W 12-Core	44	33	13
	E5-2670 v3	120W 12-Core	44	33	13
	E5-2660 v3	105W 10-Core	38	30	13
	E5-2650 v3	105W 10-Core	43	33	13
Standard Server	E5-2640 v3	90W 8-Core	33	25	12
	E5-2630 v3	85W 8-Core	34	26	12
	E5-2620 v3	85W 6-Core	36	28	12
Basic	E5-2609 v3	85W 6-Core	28	24	20
	E5-2603 v3	85W 6-Core	28	24	20
Low Power	E5-2650L v3	65W 12-Core	38	38	13
	E5-2630L v3	55W 8-Core	27	23	13
Embedded	E5-2663 v3	120W 10-Core	34	28	13
	E5-2658 v3	105W 12-Core	39	30	13
	E5-2628 v3	85W 8-Core	33	25	12
	E5-2648L v3	75W 12-Core	36	28	13
	E5-2628L v3	75W 10-Core	33	27	13
	E5-2618L v3	75W 8-Core	29	24	12
	E5-2608L v3	52W 6-Core	26	22	12

Notes: 1. Package C6 power specified at Tcase = 50°C.
2. Characterized but not tested.

Segment	Model Number	TDP	C1E (W) [3]	C3 (W) [3]	C6 (W)
Segment Optimized	E5-2699 v3	145W 18-Core	56	36	14
	E5-2698 v3	135W 16-Core	47	33	14
	E5-2697 v3	145W 14-Core	45	34	14
	E5-2695 v3	120W 14-Core	46	34	14
	E5-2683 v3	120W 14-Core	55	38	20
Workstation	E5-2687 v3	160W 10-Core	41	31	13
	E5-1680 v3	140W 8-Core	34	25	12
	E5-1660 v3	140W 8-Core	34	25	12
	E5-1650 v3	140W 6-Core	30	22	12
	E5-1630 v3	140W 4-Core	26	20	12
	E5-1620 v3	140W 4-Core	26	20	12
Frequency Optimized	E5-2667 v3	135W 8-Core	32	26	12
	E5-2643 v3	135W 6-Core	32	26	12
	E5-2637 v3	135W 4-Core	30	25	12
	E5-2623 v3	105W 4-Core	33	26	12
Advanced Server	E5-2690 v3	135W 12-Core	38	30	13
	E5-2680 v3	120W 12-Core	44	33	13
	E5-2670 v3	120W 12-Core	44	33	13
	E5-2660 v3	105W 10-Core	38	30	13
	E5-2650 v3	105W 10-Core	43	33	13
Standard Server	E5-2640 v3	90W 8-Core	33	25	12
	E5-2630 v3	85W 8-Core	34	26	12
	E5-2620 v3	85W 6-Core	36	28	12
Basic	E5-2609 v3	85W 6-Core	28	24	20
	E5-2603 v3	85W 6-Core	28	24	20
Low Power	E5-2650L v3	65W 12-Core	38	38	13
	E5-2630L v3	55W 8-Core	27	23	13
Embedded	E5-2663 v3	120W 10-Core	34	28	13
	E5-2658 v3	105W 12-Core	39	30	13
	E5-2628 v3	85W 8-Core	33	25	12
	E5-2648L v3	75W 12-Core	36	28	13
	E5-2628L v3	75W 10-Core	33	27	13
	E5-2618L v3	75W 8-Core	29	24	12

continued...



Segment	Model Number	TDP	C1E (W) [3]	C3 (W) [3]	C6 (W)
	E5-2608L v3	52W 6-Core	26	22	12

Notes: 1. SKUs are subject to change. Contact your Intel Field Representative to obtain the latest SKU information.
2. Package C6 power specified at Tcase = 50°C.
3. Characterized but not tested.

2.11 Signal Quality

Data transfer requires the clean reception of data signals and clock signals. Ringing below receiver thresholds, non-monotonic signal edges, and excessive voltage swings will adversely affect system timings. Ringback and signal non-monotonicity cannot be tolerated since these phenomena may inadvertently advance receiver state machines. Excessive signal swings (overshoot and undershoot) are detrimental to silicon gate oxide integrity, and can cause device failure if absolute voltage limits are exceeded. Overshoot and undershoot can also cause timing degradation due to the build up of inter-symbol interference (ISI) effects.

For these reasons, it is crucial that the designer work towards a solution that provides acceptable signal quality across all systematic variations encountered in volume manufacturing.

This section documents signal quality metrics used to derive topology and routing guidelines through simulation. All specifications are specified at the processor die (pad measurements).

Specifications for signal quality are for measurements at the processor core only and are only observable through simulation. Therefore, proper simulation is the only way to verify proper timing and signal quality.

2.11.1 DDR Signal Quality Specifications

Overshoot (or undershoot) is the absolute value of the maximum voltage above or below VSS. The overshoot/undershoot specifications limit transitions beyond specified maximum voltages or VSS due to the fast signal edge rates. The processor can be damaged by single and/or repeated overshoot or undershoot events on any input, output, or I/O buffer if the charge is large enough (i.e., if the over/undershoot is great enough). Baseboard designs which meet signal integrity and timing requirements and which do not exceed the maximum overshoot or undershoot limits listed in Table 17 on page 46 will ensure reliable IO performance for the lifetime of the processor.

2.11.2 I/O Signal Quality Specifications

Signal Quality specifications for PCIe* Signals are included as part of the PCIe DC specifications.

2.11.3 Input Reference Clock Signal Quality Specifications

Overshoot/Undershoot and Ringback specifications for BCLK{0/1}_D[N/P] are found in Table 17 on page 46. Overshoot/Undershoot and Ringback specifications for the DDR4 Reference Clocks are specified by the DIMM.

2.11.4 Overshoot/Undershoot Tolerance

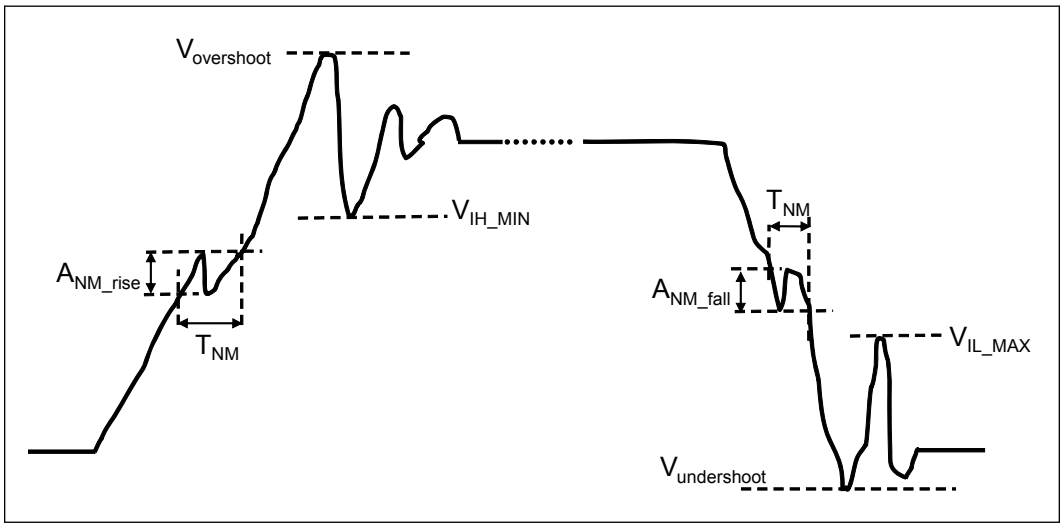
Overshoot (or undershoot) is the absolute value of the maximum voltage above or below VSS, see Figure 11 on page 47. The overshoot/undershoot specifications limit transitions beyond VCCD or VSS due to the fast signal edge rates. The processor can be damaged by single and/or repeated overshoot or undershoot events on any input, output, or I/O buffer if the charge is large enough (i.e., if the over/undershoot is great enough). Baseboard designs which meet signal integrity and timing requirements and which do not exceed the maximum overshoot or undershoot limits listed in the following table will insure reliable IO performance for the lifetime of the processor.

Table 17. Processor I/O Overshoot/Undershoot Specifications

Signal Group	Maximum Undershoot	Maximum Overshoot	Overshoot Duration	Undershoot Duration	Notes
Intel QuickPath Interconnect	-0.2 * V_{CCIO_IN}	1.2 * V_{CCIO_IN}	39 ps	15 ps	1, 2
DDR4	-0.22*V_{CCD}	1.22*V_{CCD}	0.25*T_{CH}	0.1*T_{CH}	1, 2, 3
Processor Asynchronous Sideband Signals	-0.35 * V_{CCIO_IN}	1.35 * V_{CCIO_IN}	1.25 ns	0.5 ns	1, 2
System Reference Clock (BCLK{0/1})	-0.3V	1.15V	N/A	N/A	1, 2
PWRGOOD Signal	-0.420V	V_{CCIO_IN} + 0.28	1.25 ns	0.5 ns	3

Notes:
1. These specifications are measured at the processor pad.
2. Refer to Figure 11 on page 47 for description of allowable Overshoot/Undershoot magnitude and duration.
3. T_{CH} is the minimum high pulse width duration.
4. For PWRGOOD DC specifications see Processor Asynchronous Sideband DC Specifications on page 42 and Figure 10 on page 46.

Figure 10. PWRGOOD Signal Waveform



Overshoot/Undershoot Magnitude

Magnitude describes the maximum potential difference between a signal and its voltage reference level. For the processor, both are referenced to VSS. It is important to note that the overshoot and undershoot conditions are separate and their impact must be determined independently.

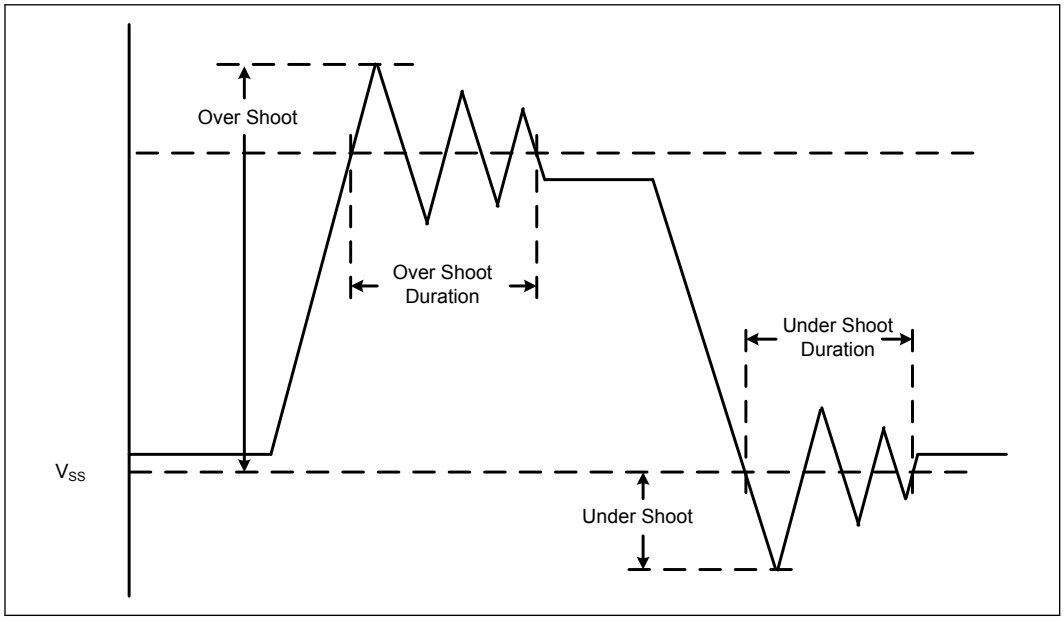
The pulse magnitude and duration must be used to determine if the overshoot/undershoot pulse is within specifications.

Overshoot/Undershoot Pulse Duration

Pulse duration describes the total amount of time that an overshoot/undershoot event exceeds the overshoot/undershoot reference voltage. The total time could encompass several oscillations above the reference voltage. Multiple overshoot/undershoot pulses within a single overshoot/undershoot event may need to be measured to determine the total pulse duration.

Note: Oscillations below the reference voltage cannot be subtracted from the total overshoot/undershoot pulse duration.

Figure 11. Maximum Acceptable Overshoot/Undershoot Waveform



Activity Factor

Activity factor (AF) describes the frequency of overshoot (or undershoot) occurrence relative to a clock. Since the highest frequency of assertion of any common clock signal is every other clock, an AF = 0.1 indicates that the specific overshoot (or undershoot) waveform occurs every other clock cycle.

The specification provided in the table shows the maximum pulse duration allowed for a given overshoot/undershoot magnitude at a specific activity factor. Each table entry is independent of all others, meaning that the pulse duration reflects the existence of overshoot/undershoot events of that magnitude ONLY. A platform with an overshoot/

undershoot that just meets the pulse duration for a specific magnitude where the AF < 0.1, means that there can be no other overshoot/undershoot events, even of lesser magnitude (note that if AF = 0.1, then the event occurs at all times and no other events can occur).

Reading Overshoot/Undershoot Specification Tables

The overshoot/undershoot specification for the processor is not a simple single value. Instead, many factors are needed to determine the over/undershoot specification. In addition to the magnitude of the overshoot, the following parameters must also be known: the width of the overshoot and the activity factor (AF). To determine the allowed overshoot for a particular overshoot event, the following must be done:

1. Determine the signal group a particular signal falls into.
2. Determine the magnitude of the overshoot or the undershoot (relative to VSS).
3. Determine the activity factor (How often does this overshoot occur?).
4. Next, from the appropriate specification table, determine the maximum pulse duration (in nanoseconds) allowed.
5. Compare the specified maximum pulse duration to the signal being measured. If the pulse duration measured is less than the pulse duration shown in the table, then the signal meets the specifications.

Undershoot events must be analyzed separately from overshoot events as they are mutually exclusive.

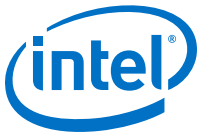
Determining if a System Meets the Overshoot/Undershoot Specifications

The overshoot/undershoot specifications listed in the table specify the allowable overshoot/undershoot for a single overshoot/undershoot event. However most systems will have multiple overshoot and/or undershoot events that each have their own set of parameters (duration, AF and magnitude). While each overshoot on its own may meet the overshoot specification, when you add the total impact of all overshoot events, the system may fail. A guideline to ensure a system passes the overshoot and undershoot specifications is shown below.

1. If only one overshoot/undershoot event magnitude occurs, ensure it meets the over/undershoot specifications in the following tables, OR
2. If multiple overshoots and/or multiple undershoots occur, measure the worst case pulse duration for each magnitude and compare the results against the AF = 0.1 specifications. If all of these worst case overshoot or undershoot events meet the specifications (measured time < specifications) in the table (where AF= 0.1), then the system passes.

Table 18. Processor Sideband Signal Group Overshoot/Undershoot Tolerance

Absolute Maximum Overshoot (V)	Absolute Maximum Undershoot (V)	Pulse Duration (ns) AF=0.1	Pulse Duration (ns) AF=0.01
1.3335 V	0.2835 V	3 ns	5 ns
1.2600 V	0.210 V	5 ns	5 ns



3.0 Processor Land Listing

Refer to Appendix A in this document.

4.0 Signal Descriptions

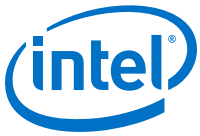
This chapter describes the Intel® Xeon® Processor E5-1600, E5-2600, and E5-4600 v3 Product Families signals. They are arranged in functional groups according to their associated interface or category.

4.1 System Memory Interface

Table 19. Memory Channel DDR0, DDR1, DDR2, DDR3

Signal Name	Description
DDR{0/1/2/3}_ACT_N	Activate. When asserted, indicates MA[16:14] are command signals (RAS_N, CAS_N, WE_N).
DDR{0/1/2/3}_ALERT_N	Parity Error detected by the DIMM (one for each channel).
DDR{0/1/2/3}_BA[1:0]	Bank Address. Defines which bank is the destination for the current Activate, Read, Write, or Precharge command.
DDR{0/1/2/3}_BG[1:0]	Bank Group: Defines which bank group is the destination for the current Active, Read, Write or Precharge command. BG0 also determines which mode register is to be accessed during a MRS cycle.
DDR{0/1/2/3}_CAS_N	Column Address Strobe. MUXed with DDR{0/1/2/3}_MA[15].
DDR{0/1/2/3}_CID[4:0]	Chip ID. Used to select a single die out of the stack of a 3DS device. CID[4:3] are MUXed with CS_N[7:6], respectively. CID[1:0] are MUXed with CS_N[3:2], respectively.
DDR{0/1/2/3}_CKE[5:0]	Clock Enable.
DDR{0/1/2/3}_CLK_DN[3:0] DDR{0/1/2/3}_CLK_DP[3:0]	Differential clocks to the DIMM. All command and control signals are valid on the rising edge of clock.
DDR{0/1/2/3}_CS_N[9:0]	Chip Select. Each signal selects one rank as the target of the command and address. CS_N[7:6] are MUXed with CID[4:3], respectively. CS_N[3:2] are MUXed with CID[1:0], respectively.
DDR{0/1/2/3}_DQ[63:0]	Data Bus. DDR4 Data bits.
DDR{0/1/2/3}_DQS_DP[17:0] DDR{0/1/2/3}_DQS_DN[17:0]	Data strobes. Differential pair, Data/ECC Strobe. Differential strobes latch data/ECC for each DRAM. Different numbers of strobes are used depending on whether the connected DRAMs are x4,x8. Driven with edges in center of data, receive edges are aligned with data edges.
DDR{0/1/2/3}_ECC[7:0]	Check bits. An error correction code is driven along with data on these lines for DIMMs that support that capability
DDR{0/1/2/3}_MA[17:0]	Memory Address. Selects the Row address for Reads and writes, and the column address for activates. Also used to set values for DRAM configuration registers. MA[16], MA[15], and MA[14] are MUXed with RAS_N, CAS_N, and WE_N, respectively.
DDR{0/1/2/3}_PAR	Even parity across Address and Command.

continued...



Signal Name	Description
DDR{0/1/2/3}_ODT[5:0]	On Die Termination. Enables DRAM on die termination during Data Write or Data Read transactions.
DDR{0/1/2/3}_RAS_N	Row Address Strobe. MUXed with DDR{0/1/2/3}_MA[16].
DDR{0/1/2/3}_WE_N	Write Enable. MUXed with DDR{0/1/2/3}_MA[14].

Table 20. Memory Channel Miscellaneous

Signal Name	Description
DDR_RESET_C01_N DDR_RESET_C23_N	System memory reset: Reset signal from processor to DRAM devices on the DIMMs. DDR_RESET_C01_N is used for memory channels 0 and 1 while DDR_RESET_C23_N is used for memory channels 2 and 3.
DDR_SCL_C01 DDR_SCL_C23	SMBus clock for the dedicated interface to the serial presence detect (SPD) and thermal sensors (TSoD) on the DIMMs. DDR_SCL_C01 is used for memory channels 0 and 1 while DDR_SCL_C23 is used for memory channels 2 and 3.
DDR_SDA_C01 DDR_SDA_C23	SMBus data for the dedicated interface to the serial presence detect (SPD) and thermal sensors (TSoD) on the DIMMs. DDR_SDA_C01 is used for memory channels 0 and 1 while DDR_SDA_C23 is used for memory channels 2 and 3.
DDR01_VREF DDR23_VREF	Voltage reference for CMD/ADD to the DIMMs. DDR01_VREF is used for memory channels 0 and 1 while DDR23_VREF is used for memory channels 2 and 3.
DRAM_PWR_OK_C01 DRAM_PWR_OK_C23	Power good for V_{CCD} rail used by the DRAM. This is an input signal used to indicate the V_{CCD} power supply is stable for memory channels 0 & 1 and channels 2 & 3.

4.2 PCI Express* Based Interface Signals

Note: PCI Express* Ports 1, 2 and 3 Signals are receive and transmit differential pairs.

Table 21. PCI Express Port 1 Signals

Signal Name	Description
PE1A_RX_DN[3:0] PE1A_RX_DP[3:0]	PCIe Receive Data Input
PE1B_RX_DN[7:4] PE1B_RX_DP[7:4]	PCIe Receive Data Input
PE1A_TX_DN[3:0] PE1A_TX_DP[3:0]	PCIe Transmit Data Output
PE1B_TX_DN[7:4] PE1B_TX_DP[7:4]	PCIe Transmit Data Output

Table 22. PCI Express Port 2 Signals

Signal Name	Description
PE2A_RX_DN[3:0] PE2A_RX_DP[3:0]	PCIe Receive Data Input
PE2B_RX_DN[7:4] PE2B_RX_DP[7:4]	PCIe Receive Data Input

continued...

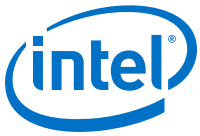
Signal Name	Description
PE2C_RX_DN[11:8] PE2C_RX_DP[11:8]	PCIe Receive Data Input
PE2D_RX_DN[15:12] PE2D_RX_DP[15:12]	PCIe Receive Data Input
PE2A_TX_DN[3:0] PE2A_TX_DP[3:0]	PCIe Transmit Data Output
PE2B_TX_DN[7:4] PE2B_TX_DP[7:4]	PCIe Transmit Data Output
PE2C_TX_DN[11:8] PE2C_TX_DP[11:8]	PCIe Transmit Data Output
PE2D_TX_DN[15:12] PE2D_TX_DP[15:12]	PCIe Transmit Data Output

Table 23. PCI Express Port 3 Signals

Signal Name	Description
PE3A_RX_DN[3:0] PE3A_RX_DP[3:0]	PCIe Receive Data Input
PE3B_RX_DN[7:4] PE3B_RX_DP[7:4]	PCIe Receive Data Input
PE3C_RX_DN[11:8] PE3C_RX_DP[11:8]	PCIe Receive Data Input
PE3D_RX_DN[15:12] PE3D_RX_DP[15:12]	PCIe Receive Data Input
PE3A_TX_DN[3:0] PE3A_TX_DP[3:0]	PCIe Transmit Data Output
PE3B_TX_DN[7:4] PE3B_TX_DP[7:4]	PCIe Transmit Data Output
PE3C_TX_DN[11:8] PE3C_TX_DP[11:8]	PCIe Transmit Data Output
PE3D_TX_DN[15:12] PE3D_TX_DP[15:12]	PCIe Transmit Data Output

Table 24. PCI Express Miscellaneous Signals

Signal Name	Description
PE_HP_SCL	PCI Express* Hot-Plug SMBus Clock: Provides PCI Express* hot-plug support via a dedicated SMBus interface. Requires an external general purpose input/output (GPIO) expansion device on the platform.
PE_HP_SDA	PCI Express* Hot-Plug SMBus Data: Provides PCI Express* hot-plug support via a dedicated SMBus interface. Requires an external general purpose input/output (GPIO) expansion device on the platform.



4.3 DMI2/PCI Express Port 0 Signals

Table 25. DMI2 and PCI Express Port 0 Signals

Signal Name	Description
DMI_RX_DN[3:0] DMI_RX_DP[3:0]	DMI2 Receive Data Input
DMI_TX_DP[3:0] DMI_TX_DN[3:0]	DMI2 Transmit Data Output

4.4 Intel® QuickPath Interconnect Signals

Table 26. Intel QPI Port 0 and 1 Signals

Signal Name	Description
QPI{0/1}_CLKRX_DN/DP	Reference Clock Differential Input. These pins provide the PLL reference clock differential input. 100 MHz typical.
QPI{0/1}_CLKTX_DN/DP	Reference Clock Differential Output. These pins provide the PLL reference clock differential input. 100 MHz typical.
QPI{0/1}_DRX_DN/DP[19:0]	QPI Receive data input.
QPI{0/1}_DTX_DN/DP[19:0]	QPI Transmit data output.

4.5 PECI Signal

Table 27. PECI Signal

Signal Name	Description
PECI	PECI (Platform Environment Control Interface) is the serial sideband interface to the processor and is used primarily for thermal, power and error management.

4.6 System Reference Clock Signals

Table 28. System Reference Clock (BCLK{0/1}) Signals

Signal Name	Description
BCLK{0/1}_D[N/P]	Reference Clock Differential input. These pins provide the required reference inputs to various PLLs inside the processor, such as Intel QPI and PCIe. BCLK0 and BCLK1 run at 100MHz from the same clock source.

4.7 JTAG and TAP Signals

Table 29. JTAG and TAP Signals

Signal Name	Description
BPM_N[7:0]	Breakpoint and Performance Monitor Signals: I/O signals from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance. These are 100 MHz signals.
PRDY_N	Probe Mode Ready is a processor output used by debug tools to determine processor debug readiness.
PREQ_N	Probe Mode Request is used by debug tools to request debug operation of the processor.
TCK	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TMS	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRST_N	TRST_N (Test Reset) resets the Test Access Port (TAP) logic. TRST_N must be driven low during power on Reset.

4.8 Serial VID Interface (SVID) Signals

Table 30. SVID Signals

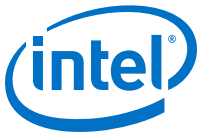
Signal Name	Description
SVIDALERT_N	Serial VID alert.
SVIDCLK	Serial VID clock.
SVIDDATA	Serial VID data out.

4.9 Processor Asynchronous Sideband and Miscellaneous Signals

Table 31. Processor Asynchronous Sideband Signals

Signal Name	Description
CATERR_N	Indicates that the system has experienced a fatal or catastrophic error and cannot continue to operate. The processor will assert CATERR_N for unrecoverable machine check errors and other internal unrecoverable errors. It is expected that every processor in the system will wire-OR CATERR_N for all processors. Since this is an I/O land, external agents are allowed to assert this land which will cause the processor to take a machine check exception. This signal is sampled after PWRGOOD assertion. On the Intel® Xeon® processor v3 product families, CATERR_N is used for signaling the following types of errors: • Legacy MCERR's, CATERR_N is asserted for 16 BCLKs. • Legacy IERR's, CATERR_N remains asserted until warm or cold reset.
ERROR_N[2:0]	Error status signals for integrated I/O (IIO) unit:

continued...



Signal Name	Description
	• 0 = Hardware correctable error (no operating system or firmware action necessary) • 1 = Non-fatal error (operating system or firmware action required to contain and recover) • 2 = Fatal error (system reset likely required to recover)
MEM_HOT_C01_N MEM_HOT_C23_N	Memory throttle control. Signals external BMC-less controller that DIMM is exceeding temperature limit and needs to increase to max fan speed. MEM_HOT_C01_N and MEM_HOT_C23_N signals have two modes of operation - input and output mode. Input mode is externally asserted and is used to detect external events such as VR_HOT# from the memory voltage regulator and causes the processor to throttle the appropriate memory channels. Output mode is asserted by the processor known as level mode. In level mode, the output indicates that a particular branch of memory subsystem is hot. MEM_HOT_C01_N is used for memory channels 0 & 1 while MEM_HOT_C23_N is used for memory channels 2 & 3.
MSMI_N	Machine Check Exception (MCE) is signaled via this pin when eMCA2 is enabled.
PMSYNC	Power Management Sync. A sideband signal to communicate power management status from the Platform Controller Hub (PCH) to the processor.
PROCHOT_N	PROCHOT_N will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit has been activated, if enabled. This signal can also be driven to the processor to activate the Thermal Control Circuit. This signal is sampled after PWRGOOD assertion on a cold boot. If PROCHOT_N is asserted at the assertion of RESET_N on a warm boot, the processor will tristate its outputs.

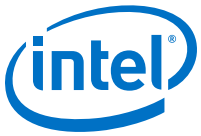
continued...

Signal Name	Description
PWRGOOD	PWRGOOD is a processor input. The processor requires this signal to be a clean indication that all processor clocks and power supplies are stable and within their specifications. "Clean" implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. PWRGOOD transitions from inactive to active when all supplies except VCCIN are stable. The signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.
RESET_N	Global reset signal. Asserting the RESET_N signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. Note some PLL, Intel QuickPath Interconnect and error states are not affected by reset and only PWRGOOD forces them to a known state.
THERMTRIP_N	Assertion of THERMTRIP_N (Thermal Trip) indicates one of two possible critical over-temperature conditions: One, the processor junction temperature has reached a level beyond which permanent silicon damage may occur and Two, the system memory interface has exceeded a critical temperature limit set by BIOS. Measurement of the processor junction temperature is accomplished through multiple internal thermal sensors that are monitored by the Digital Thermal Sensor (DTS). Simultaneously, the Power Control Unit (PCU) monitors external memory temperatures via the dedicated SMBus interface to the DIMMs. If any of the DIMMs exceed the BIOS defined limits, the PCU will signal THERMTRIP_N to prevent damage to the DIMMs. Once activated, the processor will stop all execution and shut down all PLLs. To further protect the processor, its core voltage (V_{CCIN}), V_{CCD}, V_{CCIO_IN}, V_{CCPECI} supplies must be removed following the assertion of THERMTRIP_N. Once activated, THERMTRIP_N remains latched until RESET_N is asserted. While the assertion of the RESET_N signal may de-assert THERMTRIP_N, if the processor's junction temperature remains at or above the trip level, THERMTRIP_N will again be asserted after RESET_N is de-asserted. This signal can also be asserted if the system memory interface has exceeded a critical temperature limit set by BIOS.

Table 32. Miscellaneous Signals

Signal Name	Description
BIST_ENABLE	BIST Enable Strap. Input which allows the platform to enable or disable built-in self test (BIST) on the processor. This signal is pulled up on the die. Rrefer to Table 8 on page 26 for details.
BMCINIT	BMC Initialization Strap. Indicates whether Service Processor Boot Mode should be used. Used in combination with FRMAGENT and SOCKET_ID inputs. • 0: Service Processor Boot Mode Disabled. Example boot modes: Local PCH (this processor hosts a legacy PCH with firmware behind it), Intel QPI Link Boot (for processors one hop away from the FW agent), or Intel QPI Link Init (for processors more than one hop away from the firmware agent). • 1: Service Processor Boot Mode Enabled. In this mode of operation, the processor performs the absolute minimum internal configuration and then waits for the Service Processor to complete its initialization. The socket boots after receiving a "GO" handshake signal via a firmware scratchpad register.

continued...



Signal Name	Description
	This signal is pulled down on the die, refer to Table 8 on page 26 for details.
EAR_N	External Alignment of Reset, used to bring the processor up into a deterministic state. This signal is pulled up on the die, refer to Table 8 on page 26 for details.
FIVR_FAULT	Indicates an internal error has occurred with the integrated voltage regulator. The FIVR_FAULT signal can be sampled any time after 1.5 ms after the assertion of PWRGOOD. FIVR_FAULT must be qualified by THERMTRIP_N assertion.
FRMAGENT	Bootable Firmware Agent Strap. This input configuration strap used in combination with SOCKET_ID to determine whether the socket is a legacy socket, bootable firmware agent is present, and DMI links are used in PCIe* mode (instead of DMI2 mode). The firmware flash ROM is located behind the local PCH attached to the processor via the DMI2 interface.This signal is pulled down on the die, refer to Table 8 on page 26 for details.
PM_FAST_WAKE_N	Power Management Fast Wake. Enables quick package C3 - C6 exits of all sockets. Asserted if any socket detects a break from package C3 - C6 state requiring all sockets to exit the low power state to service a snoop, memory access, or interrupt. Expected to be wired-OR among all processor sockets within the platform.
PROC_ID	This output can be used by the platform to determine if the installed processor is a Intel® Xeon® processor E5-1600 and E5-2600 v3 product families. There is no connection to the processor silicon for this signal. The processor package grounds or floats the pin to set '0' or '1', respectively. 1: Intel® Xeon® processor E5-1600 and E5-2600 v3 product families 0: Reserved for future use.
RSVD	RESERVED. All signals that are RSVD must be left unconnected on the board. Refer to Reserved or Unused Signals on page 22 for details.
SAFE_MODE_BOOT	Safe Mode Boot Strap. SAFE_MODE_BOOT allows the processor to wake up safely by disabling all clock gating. This allows BIOS to load registers or patches if required. This signal is sampled after PWRGOOD assertion. The signal is pulled down on the die. Refer to Table 8 on page 26 for details.
SKTOCC_N	SKTOCC_N (Socket Occupied) is used to indicate that a processor is present. This is pulled to ground on the processor package; there is no connection to the processor silicon for this signal.
SOCKET_ID[1:0]	Socket ID Strap. Socket identification configuration straps for establishing the PECI address, Intel® QPI Node ID, and other settings. This signal is used in combination with FRMAGENT to determine whether the socket is a legacy socket, bootable firmware agent is present, and DMI links are used in PCIe* mode (instead of DMI2 mode). Each processor socket consumes one Node ID, and there are 128 Home Agent tracker entries. This signal is pulled down on the die. Refer to Table 8 on page 26 for details.
TEST[3:0]	Test[3:0] must be individually connected to an appropriate power source or ground through a resistor for proper processor operation.
TXT_AGENT	Intel® Trusted Execution Technology (Intel® TXT) Agent Strap. 0 = Default. The socket is not the Intel TXT Agent. 1 = The socket is the Intel TXT Agent. The legacy socket (identified by SOCKET_ID[1:0] = 00b) with Intel TXT Agent should always set the TXT_AGENT to 1b. This signal is pulled down on the die, refer to Table 8 on page 26 for details.
TXT_PLTEN	Intel Trusted Execution Technology (Intel TXT) Platform Enable Strap. 0 = The platform is not Intel TXT enabled. All sockets should be set to zero. Scalable DP (sDP) platforms should choose this setting if the Node Controller does not support Intel TXT.

Signal Name	Description
	1 = Default. The platform is Intel TXT enabled. All sockets should be set to one. In a non-Scalable DP platform this is the default. When this is set, Intel TXT functionality requires user to explicitly enable Intel TXT via BIOS setup. This signal is pulled up on the die, refer to Table 8 on page 26 for details.

4.10 Processor Power and Ground Supplies

Table 33. Power and Ground Signals

Signal Name	Description
V_{CCIN}	Input to the Integrated Voltage Regulator (IVR) for the processor cores, lowest level caches (LLC), ring interface, PLL, IO, and home agent. It is provided by a VR 12.5 compliant motherboard voltage regulator (MBVR) for each CPU socket. The output voltage of this MBVR is controlled by the processor, using the serial voltage ID (SVID) bus.
V_{CCIN_SENSE} $V_{SS\_VCCIN\_SENSE}$	V_{CCIN_SENSE} and $V_{SS\_VCCIN\_SENSE}$ are remote sense signals for V_{CCIN} MBVR12.5 and are used by the voltage regulator to ensure accurate voltage regulation. These signals must be connected to the voltage regulator feedback circuit, which ensures the output voltage remains within specification.
V_{CCD_01} V_{CCD_23}	Fixed 1.2V power supply for the processor system memory interface. Provided by two MBVR 12.0 or 12.5 compliant regulators per CPU socket. V_{CCD_01} and V_{CCD_23} are used for memory channels 0 &1 and 2 & 3, respectively. The valid voltage of this supply (1.20V) is configured by BIOS after determining the operating voltages of the installed memory. V_{CCD_01} and V_{CCD_23} will also be referred to as V_{CCD}. *Note:* The processor must be provided V_{CCD_01} and V_{CCD_23} for proper operation, even in configurations where no memory is populated. A MBVR 12.0 or 12.5 controller is required.
V_{SS}	Processor ground return.
V_{CCIO_IN}	IO voltage supply input.
V_{CCPECI}	Power supply for PECI.

Appendix A: Pin List

	Pin Name	Pin Number	Buffer Type	Direction
1	BCLK0_DN	CN41	CMOS	I
2	BCLK0_DP	CL41	CMOS	I
3	BCLK1_DN	AW45	CMOS	I
4	BCLK1_DP	BA45	CMOS	I
5	BIST_ENABLE	AJ43	CMOS	I
6	BMCINIT	AM48	CMOS	I
7	BPM_N[0]	BC43	ODCMOS	I/O
8	BPM_N[1]	BB44	ODCMOS	I/O
9	BPM_N[2]	BE47	ODCMOS	I/O
10	BPM_N[3]	BF46	ODCMOS	I/O
11	BPM_N[4]	BE45	ODCMOS	I/O
12	BPM_N[5]	BD46	ODCMOS	I/O
13	BPM_N[6]	BA43	ODCMOS	I/O
14	BPM_N[7]	AW43	ODCMOS	I/O
15	CATERR_N	CC51	ODCMOS	I/O
16	DDR_RESET_C01_N	DC15	CMOS	O
17	DDR_RESET_C23_N	C23	CMOS	O
18	DDR_SCL_C01	CK42	ODCMOS	I/O
19	DDR_SCL_C23	V40	ODCMOS	I/O
20	DDR_SDA_C01	CM42	ODCMOS	I/O
21	DDR_SDA_C23	Y40	ODCMOS	I/O
22	DDR0_ACT_N	CK16	SSTL	O
23	DDR0_ALERT_N	CD16	SSTL	I
24	DDR0_BA[0]	CL21	SSTL	O
25	DDR0_BA[1]	CH20	SSTL	O
26	DDR0_BG[0]	CL17	SSTL	O
27	DDR0_BG[1]	CN17	SSTL	O
28	DDR0_CID[2]	CJ25	SSTL	O
29	DDR0_CKE[0]	CJ17	SSTL	O
30	DDR0_CKE[1]	CE17	SSTL	O
31	DDR0_CKE[2]	CF16	SSTL	O
32	DDR0_CKE[3]	CC17	SSTL	O
33	DDR0_CKE[4]	CN15	SSTL	O
34	DDR0_CKE[5]	CC15	SSTL	O
35	DDR0_CLK_DN[0]	CE21	SSTL	O
36	DDR0_CLK_DN[1]	CF18	SSTL	O
37	DDR0_CLK_DN[2]	CF20	SSTL	O
38	DDR0_CLK_DN[3]	CE19	SSTL	O
39	DDR0_CLK_DP[0]	CC21	SSTL	O
40	DDR0_CLK_DP[1]	CD18	SSTL	O
41	DDR0_CLK_DP[2]	CD20	SSTL	O
42	DDR0_CLK_DP[3]	CC19	SSTL	O
43	DDR0_CS_N[0]	CD22	SSTL	O
44	DDR0_CS_N[1]	CH22	SSTL	O
45	DDR0_CS_N[2]/CID[0]	CF26	SSTL	O

46	DDR0_CS_N[3]/CID[1]	CC25	SSTL	O
47	DDR0_CS_N[4]	CK22	SSTL	O
48	DDR0_CS_N[5]	CH24	SSTL	O
49	DDR0_CS_N[6]/CID[3]	CH26	SSTL	O
50	DDR0_CS_N[7]/CID[4]	CD26	SSTL	O
51	DDR0_CS_N[8]	CK24	SSTL	O
52	DDR0_CS_N[9]	CK26	SSTL	O
53	DDR0_DQ[0]	BU7	SSTL	I/O
54	DDR0_DQ[1]	BT6	SSTL	I/O
55	DDR0_DQ[10]	BW13	SSTL	I/O
56	DDR0_DQ[11]	BY14	SSTL	I/O
57	DDR0_DQ[12]	BT14	SSTL	I/O
58	DDR0_DQ[13]	BU15	SSTL	I/O
59	DDR0_DQ[14]	CA11	SSTL	I/O
60	DDR0_DQ[15]	BY12	SSTL	I/O
61	DDR0_DQ[16]	CE9	SSTL	I/O
62	DDR0_DQ[17]	CF8	SSTL	I/O
63	DDR0_DQ[18]	CK10	SSTL	I/O
64	DDR0_DQ[19]	CJ11	SSTL	I/O
65	DDR0_DQ[2]	CA9	SSTL	I/O
66	DDR0_DQ[20]	CD10	SSTL	I/O
67	DDR0_DQ[21]	CE11	SSTL	I/O
68	DDR0_DQ[22]	CK8	SSTL	I/O
69	DDR0_DQ[23]	CJ9	SSTL	I/O
70	DDR0_DQ[24]	CE13	SSTL	I/O
71	DDR0_DQ[25]	CG15	SSTL	I/O
72	DDR0_DQ[26]	CM14	SSTL	I/O
73	DDR0_DQ[27]	CH14	SSTL	I/O
74	DDR0_DQ[28]	CC13	SSTL	I/O
75	DDR0_DQ[29]	CD14	SSTL	I/O
76	DDR0_DQ[3]	CB8	SSTL	I/O
77	DDR0_DQ[30]	CM12	SSTL	I/O
78	DDR0_DQ[31]	CL13	SSTL	I/O
79	DDR0_DQ[32]	CK28	SSTL	I/O
80	DDR0_DQ[33]	CH28	SSTL	I/O
81	DDR0_DQ[34]	CK32	SSTL	I/O
82	DDR0_DQ[35]	CH32	SSTL	I/O
83	DDR0_DQ[36]	CL27	SSTL	I/O
84	DDR0_DQ[37]	CJ27	SSTL	I/O
85	DDR0_DQ[38]	CL31	SSTL	I/O
86	DDR0_DQ[39]	CJ31	SSTL	I/O
87	DDR0_DQ[4]	BT8	SSTL	I/O
88	DDR0_DQ[40]	CD28	SSTL	I/O
89	DDR0_DQ[41]	CB28	SSTL	I/O
90	DDR0_DQ[42]	CD32	SSTL	I/O
91	DDR0_DQ[43]	CB32	SSTL	I/O
92	DDR0_DQ[44]	CE27	SSTL	I/O
93	DDR0_DQ[45]	CC27	SSTL	I/O
94	DDR0_DQ[46]	CE31	SSTL	I/O

95	DDR0_DQ[47]	CC31	SSTL	I/O
96	DDR0_DQ[48]	CE35	SSTL	I/O
97	DDR0_DQ[49]	CC35	SSTL	I/O
98	DDR0_DQ[5]	BU9	SSTL	I/O
99	DDR0_DQ[50]	CE39	SSTL	I/O
100	DDR0_DQ[51]	CC39	SSTL	I/O
101	DDR0_DQ[52]	CF34	SSTL	I/O
102	DDR0_DQ[53]	CD34	SSTL	I/O
103	DDR0_DQ[54]	CF38	SSTL	I/O
104	DDR0_DQ[55]	CD38	SSTL	I/O
105	DDR0_DQ[56]	CL35	SSTL	I/O
106	DDR0_DQ[57]	CJ35	SSTL	I/O
107	DDR0_DQ[58]	CL39	SSTL	I/O
108	DDR0_DQ[59]	CJ39	SSTL	I/O
109	DDR0_DQ[6]	CA7	SSTL	I/O
110	DDR0_DQ[60]	CM34	SSTL	I/O
111	DDR0_DQ[61]	CK34	SSTL	I/O
112	DDR0_DQ[62]	CM38	SSTL	I/O
113	DDR0_DQ[63]	CK38	SSTL	I/O
114	DDR0_DQ[7]	CB6	SSTL	I/O
115	DDR0_DQ[8]	BT12	SSTL	I/O
116	DDR0_DQ[9]	BU11	SSTL	I/O
117	DDR0_DQS_DN[0]	BV6	SSTL	I/O
118	DDR0_DQS_DN[1]	BW11	SSTL	I/O
119	DDR0_DQS_DN[10]	BV14	SSTL	I/O
120	DDR0_DQS_DN[11]	CH8	SSTL	I/O
121	DDR0_DQS_DN[12]	CF14	SSTL	I/O
122	DDR0_DQS_DN[13]	CJ29	SSTL	I/O
123	DDR0_DQS_DN[14]	CC29	SSTL	I/O
124	DDR0_DQS_DN[15]	CD36	SSTL	I/O
125	DDR0_DQS_DN[16]	CK36	SSTL	I/O
126	DDR0_DQS_DN[17]	CW9	SSTL	I/O
127	DDR0_DQS_DN[2]	CG11	SSTL	I/O
128	DDR0_DQS_DN[3]	CJ13	SSTL	I/O
129	DDR0_DQS_DN[4]	CM30	SSTL	I/O
130	DDR0_DQS_DN[5]	CF30	SSTL	I/O
131	DDR0_DQS_DN[6]	CE37	SSTL	I/O
132	DDR0_DQS_DN[7]	CL37	SSTL	I/O
133	DDR0_DQS_DN[8]	CT10	SSTL	I/O
134	DDR0_DQS_DN[9]	BW9	SSTL	I/O
135	DDR0_DQS_DP[0]	BY6	SSTL	I/O
136	DDR0_DQS_DP[1]	BV12	SSTL	I/O
137	DDR0_DQS_DP[10]	BU13	SSTL	I/O
138	DDR0_DQS_DP[11]	CG9	SSTL	I/O
139	DDR0_DQS_DP[12]	CG13	SSTL	I/O
140	DDR0_DQS_DP[13]	CL29	SSTL	I/O
141	DDR0_DQS_DP[14]	CE29	SSTL	I/O
142	DDR0_DQS_DP[15]	CF36	SSTL	I/O
143	DDR0_DQS_DP[16]	CM36	SSTL	I/O

144	DDR0_DQS_DP[17]	CU9	SSTL	I/O
145	DDR0_DQS_DP[2]	CH10	SSTL	I/O
146	DDR0_DQS_DP[3]	CK14	SSTL	I/O
147	DDR0_DQS_DP[4]	CK30	SSTL	I/O
148	DDR0_DQS_DP[5]	CD30	SSTL	I/O
149	DDR0_DQS_DP[6]	CC37	SSTL	I/O
150	DDR0_DQS_DP[7]	CJ37	SSTL	I/O
151	DDR0_DQS_DP[8]	CV10	SSTL	I/O
152	DDR0_DQS_DP[9]	BV8	SSTL	I/O
153	DDR0_ECC[0]	CT8	SSTL	I/O
154	DDR0_ECC[1]	CV8	SSTL	I/O
155	DDR0_ECC[2]	CW11	SSTL	I/O
156	DDR0_ECC[3]	CU11	SSTL	I/O
157	DDR0_ECC[4]	CP8	SSTL	I/O
158	DDR0_ECC[5]	CN9	SSTL	I/O
159	DDR0_ECC[6]	CP10	SSTL	I/O
160	DDR0_ECC[7]	CR11	SSTL	I/O
161	DDR0_MA[0]	CP22	SSTL	O
162	DDR0_MA[1]	CR21	SSTL	O
163	DDR0_MA[10]	CP24	SSTL	O
164	DDR0_MA[11]	CP18	SSTL	O
165	DDR0_MA[12]	CR17	SSTL	O
166	DDR0_MA[13]	CE23	SSTL	O
167	DDR0_MA[14]	CJ21	SSTL	O
168	DDR0_MA[15]	CL25	SSTL	O
169	DDR0_MA[16]	CL23	SSTL	O
170	DDR0_MA[17]	CD24	SSTL	O
171	DDR0_MA[2]	CT22	SSTL	O
172	DDR0_MA[3]	CN21	SSTL	O
173	DDR0_MA[4]	CP20	SSTL	O
174	DDR0_MA[5]	CL19	SSTL	O
175	DDR0_MA[6]	CN19	SSTL	O
176	DDR0_MA[7]	CH18	SSTL	O
177	DDR0_MA[8]	CJ19	SSTL	O
178	DDR0_MA[9]	CK18	SSTL	O
179	DDR0_ODT[0]	CF22	SSTL	O
180	DDR0_ODT[1]	CN25	SSTL	O
181	DDR0_ODT[2]	CJ23	SSTL	O
182	DDR0_ODT[3]	CC23	SSTL	O
183	DDR0_ODT[4]	CF24	SSTL	O
184	DDR0_ODT[5]	CE25	SSTL	O
185	DDR0_PAR	CK20	SSTL	O
186	DDR01_VREF	BY16	DC	O
187	DDR1_ACT_N	CT16	SSTL	O
188	DDR1_ALERT_N	CR15	SSTL	I
189	DDR1_BA[0]	CW23	SSTL	O
190	DDR1_BA[1]	CV22	SSTL	O
191	DDR1_BG[0]	CV16	SSTL	O
192	DDR1_BG[1]	CP16	SSTL	O

193	DDR1_CID[2]	CR25	SSTL	O
194	DDR1_CKE[0]	DA17	SSTL	O
195	DDR1_CKE[1]	DC17	SSTL	O
196	DDR1_CKE[2]	DD16	SSTL	O
197	DDR1_CKE[3]	DF16	SSTL	O
198	DDR1_CKE[4]	CY16	SSTL	O
199	DDR1_CKE[5]	DA15	SSTL	O
200	DDR1_CLK_DN[0]	DC21	SSTL	O
201	DDR1_CLK_DN[1]	DD18	SSTL	O
202	DDR1_CLK_DN[2]	DD20	SSTL	O
203	DDR1_CLK_DN[3]	DC19	SSTL	O
204	DDR1_CLK_DP[0]	DE21	SSTL	O
205	DDR1_CLK_DP[1]	DF18	SSTL	O
206	DDR1_CLK_DP[2]	DF20	SSTL	O
207	DDR1_CLK_DP[3]	DE19	SSTL	O
208	DDR1_CS_N[0]	DF22	SSTL	O
209	DDR1_CS_N[1]	DE23	SSTL	O
210	DDR1_CS_N[2]/CID[0]	CT26	SSTL	O
211	DDR1_CS_N[3]/CID[1]	CP26	SSTL	O
212	DDR1_CS_N[4]	DA23	SSTL	O
213	DDR1_CS_N[5]	DD24	SSTL	O
214	DDR1_CS_N[6]/CID[3]	CY26	SSTL	O
215	DDR1_CS_N[7]/CID[4]	CV26	SSTL	O
216	DDR1_CS_N[8]	DF24	SSTL	O
217	DDR1_CS_N[9]	DF26	SSTL	O
218	DDR1_DQ[0]	BV4	SSTL	I/O
219	DDR1_DQ[1]	BU1	SSTL	I/O
220	DDR1_DQ[10]	CL5	SSTL	I/O
221	DDR1_DQ[11]	CM4	SSTL	I/O
222	DDR1_DQ[12]	CE5	SSTL	I/O
223	DDR1_DQ[13]	CF6	SSTL	I/O
224	DDR1_DQ[14]	CK6	SSTL	I/O
225	DDR1_DQ[15]	CL3	SSTL	I/O
226	DDR1_DQ[16]	CR3	SSTL	I/O
227	DDR1_DQ[17]	CV2	SSTL	I/O
228	DDR1_DQ[18]	CT6	SSTL	I/O
229	DDR1_DQ[19]	CP6	SSTL	I/O
230	DDR1_DQ[2]	CA3	SSTL	I/O
231	DDR1_DQ[20]	CR1	SSTL	I/O
232	DDR1_DQ[21]	CP2	SSTL	I/O
233	DDR1_DQ[22]	CU5	SSTL	I/O
234	DDR1_DQ[23]	CR5	SSTL	I/O
235	DDR1_DQ[24]	DA7	SSTL	I/O
236	DDR1_DQ[25]	DB8	SSTL	I/O
237	DDR1_DQ[26]	DE11	SSTL	I/O
238	DDR1_DQ[27]	DC11	SSTL	I/O
239	DDR1_DQ[28]	DA5	SSTL	I/O
240	DDR1_DQ[29]	CY6	SSTL	I/O
241	DDR1_DQ[3]	CB4	SSTL	I/O

242	DDR1_DQ[30]	DE9	SSTL	I/O
243	DDR1_DQ[31]	DF10	SSTL	I/O
244	DDR1_DQ[32]	CT28	SSTL	I/O
245	DDR1_DQ[33]	CP28	SSTL	I/O
246	DDR1_DQ[34]	CT32	SSTL	I/O
247	DDR1_DQ[35]	CP32	SSTL	I/O
248	DDR1_DQ[36]	CU27	SSTL	I/O
249	DDR1_DQ[37]	CR27	SSTL	I/O
250	DDR1_DQ[38]	CU31	SSTL	I/O
251	DDR1_DQ[39]	CR31	SSTL	I/O
252	DDR1_DQ[4]	BT4	SSTL	I/O
253	DDR1_DQ[40]	DA29	SSTL	I/O
254	DDR1_DQ[41]	DB30	SSTL	I/O
255	DDR1_DQ[42]	DC33	SSTL	I/O
256	DDR1_DQ[43]	DF34	SSTL	I/O
257	DDR1_DQ[44]	DB28	SSTL	I/O
258	DDR1_DQ[45]	CY28	SSTL	I/O
259	DDR1_DQ[46]	DA33	SSTL	I/O
260	DDR1_DQ[47]	DE33	SSTL	I/O
261	DDR1_DQ[48]	CU35	SSTL	I/O
262	DDR1_DQ[49]	CR35	SSTL	I/O
263	DDR1_DQ[5]	BT2	SSTL	I/O
264	DDR1_DQ[50]	CU39	SSTL	I/O
265	DDR1_DQ[51]	CR39	SSTL	I/O
266	DDR1_DQ[52]	CV34	SSTL	I/O
267	DDR1_DQ[53]	CT34	SSTL	I/O
268	DDR1_DQ[54]	CV38	SSTL	I/O
269	DDR1_DQ[55]	CT38	SSTL	I/O
270	DDR1_DQ[56]	DC37	SSTL	I/O
271	DDR1_DQ[57]	DF36	SSTL	I/O
272	DDR1_DQ[58]	DC39	SSTL	I/O
273	DDR1_DQ[59]	DA39	SSTL	I/O
274	DDR1_DQ[6]	CA1	SSTL	I/O
275	DDR1_DQ[60]	DC35	SSTL	I/O
276	DDR1_DQ[61]	DB36	SSTL	I/O
277	DDR1_DQ[62]	DF38	SSTL	I/O
278	DDR1_DQ[63]	DE39	SSTL	I/O
279	DDR1_DQ[7]	BY2	SSTL	I/O
280	DDR1_DQ[8]	CE3	SSTL	I/O
281	DDR1_DQ[9]	CF4	SSTL	I/O
282	DDR1_DQS_DN[0]	BW3	SSTL	I/O
283	DDR1_DQS_DN[1]	CH6	SSTL	I/O
284	DDR1_DQS_DN[10]	CG3	SSTL	I/O
285	DDR1_DQS_DN[11]	CU3	SSTL	I/O
286	DDR1_DQS_DN[12]	DD8	SSTL	I/O
287	DDR1_DQS_DN[13]	CR29	SSTL	I/O
288	DDR1_DQS_DN[14]	CY32	SSTL	I/O
289	DDR1_DQS_DN[15]	CT36	SSTL	I/O
290	DDR1_DQS_DN[16]	DE37	SSTL	I/O

291	DDR1_DQS_DN[17]	CY14	SSTL	I/O
292	DDR1_DQS_DN[2]	CV4	SSTL	I/O
293	DDR1_DQS_DN[3]	DC9	SSTL	I/O
294	DDR1_DQS_DN[4]	CV30	SSTL	I/O
295	DDR1_DQS_DN[5]	DB32	SSTL	I/O
296	DDR1_DQS_DN[6]	CU37	SSTL	I/O
297	DDR1_DQS_DN[7]	DA37	SSTL	I/O
298	DDR1_DQS_DN[8]	DA13	SSTL	I/O
299	DDR1_DQS_DN[9]	BW1	SSTL	I/O
300	DDR1_DQS_DP[0]	BY4	SSTL	I/O
301	DDR1_DQS_DP[1]	CJ5	SSTL	I/O
302	DDR1_DQS_DP[10]	CH4	SSTL	I/O
303	DDR1_DQS_DP[11]	CW3	SSTL	I/O
304	DDR1_DQS_DP[12]	DC7	SSTL	I/O
305	DDR1_DQS_DP[13]	CU29	SSTL	I/O
306	DDR1_DQS_DP[14]	DA31	SSTL	I/O
307	DDR1_DQS_DP[15]	CV36	SSTL	I/O
308	DDR1_DQS_DP[16]	DD36	SSTL	I/O
309	DDR1_DQS_DP[17]	CW13	SSTL	I/O
310	DDR1_DQS_DP[2]	CT4	SSTL	I/O
311	DDR1_DQS_DP[3]	DB10	SSTL	I/O
312	DDR1_DQS_DP[4]	CT30	SSTL	I/O
313	DDR1_DQS_DP[5]	DD32	SSTL	I/O
314	DDR1_DQS_DP[6]	CR37	SSTL	I/O
315	DDR1_DQS_DP[7]	DB38	SSTL	I/O
316	DDR1_DQS_DP[8]	DB14	SSTL	I/O
317	DDR1_DQS_DP[9]	BV2	SSTL	I/O
318	DDR1_ECC[0]	CU13	SSTL	I/O
319	DDR1_ECC[1]	CV14	SSTL	I/O
320	DDR1_ECC[2]	DD14	SSTL	I/O
321	DDR1_ECC[3]	DF14	SSTL	I/O
322	DDR1_ECC[4]	CR13	SSTL	I/O
323	DDR1_ECC[5]	CT14	SSTL	I/O
324	DDR1_ECC[6]	DC13	SSTL	I/O
325	DDR1_ECC[7]	DE13	SSTL	I/O
326	DDR1_MA[0]	CY22	SSTL	O
327	DDR1_MA[1]	DA21	SSTL	O
328	DDR1_MA[10]	CR23	SSTL	O
329	DDR1_MA[11]	CV18	SSTL	O
330	DDR1_MA[12]	CW17	SSTL	O
331	DDR1_MA[13]	CW25	SSTL	O
332	DDR1_MA[14]	CN23	SSTL	O
333	DDR1_MA[15]	CV24	SSTL	O
334	DDR1_MA[16]	CY24	SSTL	O
335	DDR1_MA[17]	CT24	SSTL	O
336	DDR1_MA[2]	CV20	SSTL	O
337	DDR1_MA[3]	CW21	SSTL	O
338	DDR1_MA[4]	CR19	SSTL	O
339	DDR1_MA[5]	CY20	SSTL	O

340	DDR1_MA[6]	CW19	SSTL	O
341	DDR1_MA[7]	CT18	SSTL	O
342	DDR1_MA[8]	DA19	SSTL	O
343	DDR1_MA[9]	CY18	SSTL	O
344	DDR1_ODT[0]	DD22	SSTL	O
345	DDR1_ODT[1]	DE25	SSTL	O
346	DDR1_ODT[2]	DC23	SSTL	O
347	DDR1_ODT[3]	DC25	SSTL	O
348	DDR1_ODT[4]	DA25	SSTL	O
349	DDR1_ODT[5]	DD26	SSTL	O
350	DDR1_PAR	CT20	SSTL	O
351	DDR2_ACT_N	AE21	SSTL	O
352	DDR2_ALERT_N	P22	SSTL	I
353	DDR2_BA[0]	M14	SSTL	O
354	DDR2_BA[1]	U17	SSTL	O
355	DDR2_BG[0]	AA21	SSTL	O
356	DDR2_BG[1]	AD20	SSTL	O
357	DDR2_CID[2]	U13	SSTL	O
358	DDR2_CKE[0]	R21	SSTL	O
359	DDR2_CKE[1]	U21	SSTL	O
360	DDR2_CKE[2]	T22	SSTL	O
361	DDR2_CKE[3]	Y22	SSTL	O
362	DDR2_CKE[4]	AB22	SSTL	O
363	DDR2_CKE[5]	AD22	SSTL	O
364	DDR2_CLK_DN[0]	W17	SSTL	O
365	DDR2_CLK_DN[1]	Y20	SSTL	O
366	DDR2_CLK_DN[2]	Y18	SSTL	O
367	DDR2_CLK_DN[3]	W19	SSTL	O
368	DDR2_CLK_DP[0]	AA17	SSTL	O
369	DDR2_CLK_DP[1]	AB20	SSTL	O
370	DDR2_CLK_DP[2]	AB18	SSTL	O
371	DDR2_CLK_DP[3]	AA19	SSTL	O
372	DDR2_CS_N[0]	AB16	SSTL	O
373	DDR2_CS_N[1]	T16	SSTL	O
374	DDR2_CS_N[2]/CID[0]	W13	SSTL	O
375	DDR2_CS_N[3]/CID[1]	AA13	SSTL	O
376	DDR2_CS_N[4]	P16	SSTL	O
377	DDR2_CS_N[5]	U15	SSTL	O
378	DDR2_CS_N[6]/CID[3]	AC13	SSTL	O
379	DDR2_CS_N[7]/CID[4]	AD16	SSTL	O
380	DDR2_CS_N[8]	AD18	SSTL	O
381	DDR2_CS_N[9]	T12	SSTL	O
382	DDR2_DQ[0]	AD38	SSTL	I/O
383	DDR2_DQ[1]	AA37	SSTL	I/O
384	DDR2_DQ[10]	V30	SSTL	I/O
385	DDR2_DQ[11]	T30	SSTL	I/O
386	DDR2_DQ[12]	U35	SSTL	I/O
387	DDR2_DQ[13]	R35	SSTL	I/O
388	DDR2_DQ[14]	T32	SSTL	I/O

389	DDR2_DQ[15]	W31	SSTL	I/O
390	DDR2_DQ[16]	AD34	SSTL	I/O
391	DDR2_DQ[17]	AB34	SSTL	I/O
392	DDR2_DQ[18]	AD30	SSTL	I/O
393	DDR2_DQ[19]	AB30	SSTL	I/O
394	DDR2_DQ[2]	R37	SSTL	I/O
395	DDR2_DQ[20]	AC35	SSTL	I/O
396	DDR2_DQ[21]	AA35	SSTL	I/O
397	DDR2_DQ[22]	AE31	SSTL	I/O
398	DDR2_DQ[23]	AC31	SSTL	I/O
399	DDR2_DQ[24]	U27	SSTL	I/O
400	DDR2_DQ[25]	R27	SSTL	I/O
401	DDR2_DQ[26]	U23	SSTL	I/O
402	DDR2_DQ[27]	R23	SSTL	I/O
403	DDR2_DQ[28]	V28	SSTL	I/O
404	DDR2_DQ[29]	T28	SSTL	I/O
405	DDR2_DQ[3]	Y38	SSTL	I/O
406	DDR2_DQ[30]	V24	SSTL	I/O
407	DDR2_DQ[31]	T24	SSTL	I/O
408	DDR2_DQ[32]	N9	SSTL	I/O
409	DDR2_DQ[33]	K8	SSTL	I/O
410	DDR2_DQ[34]	R7	SSTL	I/O
411	DDR2_DQ[35]	P6	SSTL	I/O
412	DDR2_DQ[36]	J9	SSTL	I/O
413	DDR2_DQ[37]	L9	SSTL	I/O
414	DDR2_DQ[38]	K6	SSTL	I/O
415	DDR2_DQ[39]	M6	SSTL	I/O
416	DDR2_DQ[4]	AE37	SSTL	I/O
417	DDR2_DQ[40]	U9	SSTL	I/O
418	DDR2_DQ[41]	W11	SSTL	I/O
419	DDR2_DQ[42]	AA11	SSTL	I/O
420	DDR2_DQ[43]	AB8	SSTL	I/O
421	DDR2_DQ[44]	T10	SSTL	I/O
422	DDR2_DQ[45]	U11	SSTL	I/O
423	DDR2_DQ[46]	AA9	SSTL	I/O
424	DDR2_DQ[47]	Y8	SSTL	I/O
425	DDR2_DQ[48]	AE11	SSTL	I/O
426	DDR2_DQ[49]	AF12	SSTL	I/O
427	DDR2_DQ[5]	AC39	SSTL	I/O
428	DDR2_DQ[50]	AK12	SSTL	I/O
429	DDR2_DQ[51]	AL13	SSTL	I/O
430	DDR2_DQ[52]	AG15	SSTL	I/O
431	DDR2_DQ[53]	AF14	SSTL	I/O
432	DDR2_DQ[54]	AK14	SSTL	I/O
433	DDR2_DQ[55]	AL15	SSTL	I/O
434	DDR2_DQ[56]	AG9	SSTL	I/O
435	DDR2_DQ[57]	AG7	SSTL	I/O
436	DDR2_DQ[58]	AK10	SSTL	I/O
437	DDR2_DQ[59]	AL9	SSTL	I/O

438	DDR2_DQ[6]	T38	SSTL	I/O
439	DDR2_DQ[60]	AE7	SSTL	I/O
440	DDR2_DQ[61]	AE9	SSTL	I/O
441	DDR2_DQ[62]	AK8	SSTL	I/O
442	DDR2_DQ[63]	AL7	SSTL	I/O
443	DDR2_DQ[7]	U37	SSTL	I/O
444	DDR2_DQ[8]	V34	SSTL	I/O
445	DDR2_DQ[9]	U33	SSTL	I/O
446	DDR2_DQS_DN[0]	W37	SSTL	I/O
447	DDR2_DQS_DN[1]	V32	SSTL	I/O
448	DDR2_DQS_DN[10]	R33	SSTL	I/O
449	DDR2_DQS_DN[11]	AA33	SSTL	I/O
450	DDR2_DQS_DN[12]	T26	SSTL	I/O
451	DDR2_DQS_DN[13]	L7	SSTL	I/O
452	DDR2_DQS_DN[14]	W9	SSTL	I/O
453	DDR2_DQS_DN[15]	AJ15	SSTL	I/O
454	DDR2_DQS_DN[16]	AJ9	SSTL	I/O
455	DDR2_DQS_DN[17]	AB26	SSTL	I/O
456	DDR2_DQS_DN[2]	AD32	SSTL	I/O
457	DDR2_DQS_DN[3]	W25	SSTL	I/O
458	DDR2_DQS_DN[4]	P8	SSTL	I/O
459	DDR2_DQS_DN[5]	Y10	SSTL	I/O
460	DDR2_DQS_DN[6]	AJ13	SSTL	I/O
461	DDR2_DQS_DN[7]	AH8	SSTL	I/O
462	DDR2_DQS_DN[8]	AE25	SSTL	I/O
463	DDR2_DQS_DN[9]	AC37	SSTL	I/O
464	DDR2_DQS_DP[0]	V38	SSTL	I/O
465	DDR2_DQS_DP[1]	U31	SSTL	I/O
466	DDR2_DQS_DP[10]	T34	SSTL	I/O
467	DDR2_DQS_DP[11]	AC33	SSTL	I/O
468	DDR2_DQS_DP[12]	V26	SSTL	I/O
469	DDR2_DQS_DP[13]	M8	SSTL	I/O
470	DDR2_DQS_DP[14]	V8	SSTL	I/O
471	DDR2_DQS_DP[15]	AH16	SSTL	I/O
472	DDR2_DQS_DP[16]	AH10	SSTL	I/O
473	DDR2_DQS_DP[17]	AD26	SSTL	I/O
474	DDR2_DQS_DP[2]	AB32	SSTL	I/O
475	DDR2_DQS_DP[3]	U25	SSTL	I/O
476	DDR2_DQS_DP[4]	N7	SSTL	I/O
477	DDR2_DQS_DP[5]	AB10	SSTL	I/O
478	DDR2_DQS_DP[6]	AH12	SSTL	I/O
479	DDR2_DQS_DP[7]	AJ7	SSTL	I/O
480	DDR2_DQS_DP[8]	AC25	SSTL	I/O
481	DDR2_DQS_DP[9]	AB38	SSTL	I/O
482	DDR2_ECC[0]	AC27	SSTL	I/O
483	DDR2_ECC[1]	AA27	SSTL	I/O
484	DDR2_ECC[2]	AC23	SSTL	I/O
485	DDR2_ECC[3]	AA23	SSTL	I/O
486	DDR2_ECC[4]	AD28	SSTL	I/O

487	DDR2_ECC[5]	AB28	SSTL	I/O
488	DDR2_ECC[6]	AD24	SSTL	I/O
489	DDR2_ECC[7]	AB24	SSTL	I/O
490	DDR2_MA[0]	L15	SSTL	O
491	DDR2_MA[1]	M16	SSTL	O
492	DDR2_MA[10]	AA15	SSTL	O
493	DDR2_MA[11]	T20	SSTL	O
494	DDR2_MA[12]	W21	SSTL	O
495	DDR2_MA[13]	P12	SSTL	O
496	DDR2_MA[14]	Y14	SSTL	O
497	DDR2_MA[15]	R13	SSTL	O
498	DDR2_MA[16]	P14	SSTL	O
499	DDR2_MA[17]	T14	SSTL	O
500	DDR2_MA[2]	T18	SSTL	O
501	DDR2_MA[3]	L17	SSTL	O
502	DDR2_MA[4]	R19	SSTL	O
503	DDR2_MA[5]	P18	SSTL	O
504	DDR2_MA[6]	M18	SSTL	O
505	DDR2_MA[7]	U19	SSTL	O
506	DDR2_MA[8]	L19	SSTL	O
507	DDR2_MA[9]	P20	SSTL	O
508	DDR2_ODT[0]	Y16	SSTL	O
509	DDR2_ODT[1]	W15	SSTL	O
510	DDR2_ODT[2]	R15	SSTL	O
511	DDR2_ODT[3]	AB14	SSTL	O
512	DDR2_ODT[4]	AE17	SSTL	O
513	DDR2_ODT[5]	AD14	SSTL	O
514	DDR2_PAR	R17	SSTL	O
515	DDR23_VREF	T40	DC	O
516	DDR3_ACT_N	L21	SSTL	O
517	DDR3_ALERT_N	M22	SSTL	I
518	DDR3_BA[0]	G13	SSTL	O
519	DDR3_BA[1]	K14	SSTL	O
520	DDR3_BG[0]	J21	SSTL	O
521	DDR3_BG[1]	G21	SSTL	O
522	DDR3_CID[2]	J11	SSTL	O
523	DDR3_CKE[0]	F22	SSTL	O
524	DDR3_CKE[1]	E21	SSTL	O
525	DDR3_CKE[2]	A21	SSTL	O
526	DDR3_CKE[3]	D22	SSTL	O
527	DDR3_CKE[4]	B22	SSTL	O
528	DDR3_CKE[5]	K22	SSTL	O
529	DDR3_CLK_DN[0]	C17	SSTL	O
530	DDR3_CLK_DN[1]	D20	SSTL	O
531	DDR3_CLK_DN[2]	D18	SSTL	O
532	DDR3_CLK_DN[3]	C19	SSTL	O
533	DDR3_CLK_DP[0]	A17	SSTL	O
534	DDR3_CLK_DP[1]	B20	SSTL	O
535	DDR3_CLK_DP[2]	B18	SSTL	O

536	DDR3_CLK_DP[3]	A19	SSTL	O
537	DDR3_CS_N[0]	B16	SSTL	O
538	DDR3_CS_N[1]	C15	SSTL	O
539	DDR3_CS_N[2]/CID[0]	F10	SSTL	O
540	DDR3_CS_N[3]/CID[1]	H10	SSTL	O
541	DDR3_CS_N[4]	A15	SSTL	O
542	DDR3_CS_N[5]	F14	SSTL	O
543	DDR3_CS_N[6]/CID[3]	G11	SSTL	O
544	DDR3_CS_N[7]/CID[4]	A11	SSTL	O
545	DDR3_CS_N[8]	B14	SSTL	O
546	DDR3_CS_N[9]	B12	SSTL	O
547	DDR3_DQ[0]	D38	SSTL	I/O
548	DDR3_DQ[1]	B38	SSTL	I/O
549	DDR3_DQ[10]	G31	SSTL	I/O
550	DDR3_DQ[11]	E31	SSTL	I/O
551	DDR3_DQ[12]	F34	SSTL	I/O
552	DDR3_DQ[13]	E35	SSTL	I/O
553	DDR3_DQ[14]	D32	SSTL	I/O
554	DDR3_DQ[15]	E33	SSTL	I/O
555	DDR3_DQ[16]	K34	SSTL	I/O
556	DDR3_DQ[17]	M34	SSTL	I/O
557	DDR3_DQ[18]	K30	SSTL	I/O
558	DDR3_DQ[19]	M30	SSTL	I/O
559	DDR3_DQ[2]	L37	SSTL	I/O
560	DDR3_DQ[20]	J35	SSTL	I/O
561	DDR3_DQ[21]	L35	SSTL	I/O
562	DDR3_DQ[22]	L31	SSTL	I/O
563	DDR3_DQ[23]	N31	SSTL	I/O
564	DDR3_DQ[24]	F28	SSTL	I/O
565	DDR3_DQ[25]	E27	SSTL	I/O
566	DDR3_DQ[26]	F24	SSTL	I/O
567	DDR3_DQ[27]	E23	SSTL	I/O
568	DDR3_DQ[28]	G29	SSTL	I/O
569	DDR3_DQ[29]	E29	SSTL	I/O
570	DDR3_DQ[3]	M38	SSTL	I/O
571	DDR3_DQ[30]	C25	SSTL	I/O
572	DDR3_DQ[31]	B24	SSTL	I/O
573	DDR3_DQ[32]	K4	SSTL	I/O
574	DDR3_DQ[33]	H4	SSTL	I/O
575	DDR3_DQ[34]	J1	SSTL	I/O
576	DDR3_DQ[35]	L1	SSTL	I/O
577	DDR3_DQ[36]	P4	SSTL	I/O
578	DDR3_DQ[37]	N3	SSTL	I/O
579	DDR3_DQ[38]	K2	SSTL	I/O
580	DDR3_DQ[39]	R3	SSTL	I/O
581	DDR3_DQ[4]	C39	SSTL	I/O
582	DDR3_DQ[40]	E9	SSTL	I/O
583	DDR3_DQ[41]	F8	SSTL	I/O
584	DDR3_DQ[42]	E5	SSTL	I/O

585	DDR3_DQ[43]	F6	SSTL	I/O
586	DDR3_DQ[44]	C9	SSTL	I/O
587	DDR3_DQ[45]	A9	SSTL	I/O
588	DDR3_DQ[46]	D6	SSTL	I/O
589	DDR3_DQ[47]	G7	SSTL	I/O
590	DDR3_DQ[48]	AG3	SSTL	I/O
591	DDR3_DQ[49]	AG1	SSTL	I/O
592	DDR3_DQ[5]	J39	SSTL	I/O
593	DDR3_DQ[50]	AL3	SSTL	I/O
594	DDR3_DQ[51]	AL5	SSTL	I/O
595	DDR3_DQ[52]	AG5	SSTL	I/O
596	DDR3_DQ[53]	AE3	SSTL	I/O
597	DDR3_DQ[54]	AJ3	SSTL	I/O
598	DDR3_DQ[55]	AL1	SSTL	I/O
599	DDR3_DQ[56]	V4	SSTL	I/O
600	DDR3_DQ[57]	W3	SSTL	I/O
601	DDR3_DQ[58]	AC5	SSTL	I/O
602	DDR3_DQ[59]	AE5	SSTL	I/O
603	DDR3_DQ[6]	G37	SSTL	I/O
604	DDR3_DQ[60]	U5	SSTL	I/O
605	DDR3_DQ[61]	V6	SSTL	I/O
606	DDR3_DQ[62]	AC3	SSTL	I/O
607	DDR3_DQ[63]	AB6	SSTL	I/O
608	DDR3_DQ[7]	K38	SSTL	I/O
609	DDR3_DQ[8]	A35	SSTL	I/O
610	DDR3_DQ[9]	B34	SSTL	I/O
611	DDR3_DQS_DN[0]	C37	SSTL	I/O
612	DDR3_DQS_DN[1]	A33	SSTL	I/O
613	DDR3_DQS_DN[10]	D34	SSTL	I/O
614	DDR3_DQS_DN[11]	L33	SSTL	I/O
615	DDR3_DQS_DN[12]	D26	SSTL	I/O
616	DDR3_DQS_DN[13]	L3	SSTL	I/O
617	DDR3_DQS_DN[14]	D8	SSTL	I/O
618	DDR3_DQS_DN[15]	AJ5	SSTL	I/O
619	DDR3_DQS_DN[16]	W5	SSTL	I/O
620	DDR3_DQS_DN[17]	K26	SSTL	I/O
621	DDR3_DQS_DN[2]	K32	SSTL	I/O
622	DDR3_DQS_DN[3]	G25	SSTL	I/O
623	DDR3_DQS_DN[4]	G3	SSTL	I/O
624	DDR3_DQS_DN[5]	C7	SSTL	I/O
625	DDR3_DQS_DN[6]	AJ1	SSTL	I/O
626	DDR3_DQS_DN[7]	AA5	SSTL	I/O
627	DDR3_DQS_DN[8]	N25	SSTL	I/O
628	DDR3_DQS_DN[9]	H38	SSTL	I/O
629	DDR3_DQS_DP[0]	E37	SSTL	I/O
630	DDR3_DQS_DP[1]	B32	SSTL	I/O
631	DDR3_DQS_DP[10]	C35	SSTL	I/O
632	DDR3_DQS_DP[11]	J33	SSTL	I/O
633	DDR3_DQS_DP[12]	F26	SSTL	I/O

634	DDR3_DQS_DP[13]	M4	SSTL	I/O
635	DDR3_DQS_DP[14]	B8	SSTL	I/O
636	DDR3_DQS_DP[15]	AH4	SSTL	I/O
637	DDR3_DQS_DP[16]	Y6	SSTL	I/O
638	DDR3_DQS_DP[17]	M26	SSTL	I/O
639	DDR3_DQS_DP[2]	M32	SSTL	I/O
640	DDR3_DQS_DP[3]	E25	SSTL	I/O
641	DDR3_DQS_DP[4]	H2	SSTL	I/O
642	DDR3_DQS_DP[5]	E7	SSTL	I/O
643	DDR3_DQS_DP[6]	AK2	SSTL	I/O
644	DDR3_DQS_DP[7]	AB4	SSTL	I/O
645	DDR3_DQS_DP[8]	L25	SSTL	I/O
646	DDR3_DQS_DP[9]	F38	SSTL	I/O
647	DDR3_ECC[0]	L27	SSTL	I/O
648	DDR3_ECC[1]	J27	SSTL	I/O
649	DDR3_ECC[2]	L23	SSTL	I/O
650	DDR3_ECC[3]	J23	SSTL	I/O
651	DDR3_ECC[4]	K28	SSTL	I/O
652	DDR3_ECC[5]	M28	SSTL	I/O
653	DDR3_ECC[6]	M24	SSTL	I/O
654	DDR3_ECC[7]	K24	SSTL	I/O
655	DDR3_MA[0]	G15	SSTL	O
656	DDR3_MA[1]	K16	SSTL	O
657	DDR3_MA[10]	L13	SSTL	O
658	DDR3_MA[11]	K20	SSTL	O
659	DDR3_MA[12]	M20	SSTL	O
660	DDR3_MA[13]	M12	SSTL	O
661	DDR3_MA[14]	K12	SSTL	O
662	DDR3_MA[15]	F12	SSTL	O
663	DDR3_MA[16]	J13	SSTL	O
664	DDR3_MA[17]	L11	SSTL	O
665	DDR3_MA[2]	F16	SSTL	O
666	DDR3_MA[3]	G17	SSTL	O
667	DDR3_MA[4]	J17	SSTL	O
668	DDR3_MA[5]	K18	SSTL	O
669	DDR3_MA[6]	F18	SSTL	O
670	DDR3_MA[7]	J19	SSTL	O
671	DDR3_MA[8]	G19	SSTL	O
672	DDR3_MA[9]	F20	SSTL	O
673	DDR3_ODT[0]	D16	SSTL	O
674	DDR3_ODT[1]	A13	SSTL	O
675	DDR3_ODT[2]	D14	SSTL	O
676	DDR3_ODT[3]	D12	SSTL	O
677	DDR3_ODT[4]	E13	SSTL	O
678	DDR3_ODT[5]	E11	SSTL	O
679	DDR3_PAR	J15	SSTL	O
680	DEBUG_EN_N	F40	CMOS	I
681	DMI_RX_DN[0]	B50	PCIEX	I
682	DMI_RX_DN[1]	C49	PCIEX	I

683	DMI_RX_DN[2]	B48	PCIEX	I
684	DMI_RX_DN[3]	C47	PCIEX	I
685	DMI_RX_DP[0]	D50	PCIEX	I
686	DMI_RX_DP[1]	E49	PCIEX	I
687	DMI_RX_DP[2]	D48	PCIEX	I
688	DMI_RX_DP[3]	E47	PCIEX	I
689	DMI_TX_DN[0]	C45	PCIEX	O
690	DMI_TX_DN[1]	B44	PCIEX	O
691	DMI_TX_DN[2]	C43	PCIEX	O
692	DMI_TX_DN[3]	B42	PCIEX	O
693	DMI_TX_DP[0]	E45	PCIEX	O
694	DMI_TX_DP[1]	D44	PCIEX	O
695	DMI_TX_DP[2]	E43	PCIEX	O
696	DMI_TX_DP[3]	D42	PCIEX	O
697	DRAM_PWR_OK_C01	CH16	CMOS	I
698	DRAM_PWR_OK_C23	W29	CMOS	I
699	EAR_N	CE53	CMOS	I
700	ERROR_N[0]	BD50	Open Drain	O
701	ERROR_N[1]	BB48	Open Drain	O
702	ERROR_N[2]	BB52	Open Drain	O
703	FIVR_FAULT	CY40	CMOS	O
704	FRMAGENT	Y48	CMOS	I
705	MEM_HOT_C01_N	CL33	Open Drain	I/O
706	MEM_HOT_C23_N	P36	Open Drain	I/O
707	MSMI_N	H52	CMOS	I/O
708	PE_HP_SCL	B46	ODCMOS	I/O
709	PE_HP_SDA	D46	ODCMOS	I/O
710	PE1A_RX_DN[0]	C51	PCIEX3	I
711	PE1A_RX_DN[1]	D52	PCIEX3	I
712	PE1A_RX_DN[2]	D54	PCIEX3	I
713	PE1A_RX_DN[3]	E55	PCIEX3	I
714	PE1A_RX_DP[0]	E51	PCIEX3	I
715	PE1A_RX_DP[1]	F52	PCIEX3	I
716	PE1A_RX_DP[2]	F54	PCIEX3	I
717	PE1A_RX_DP[3]	G55	PCIEX3	I
718	PE1A_TX_DN[0]	H42	PCIEX3	O
719	PE1A_TX_DN[1]	J43	PCIEX3	O
720	PE1A_TX_DN[2]	H44	PCIEX3	O
721	PE1A_TX_DN[3]	J45	PCIEX3	O
722	PE1A_TX_DP[0]	K42	PCIEX3	O
723	PE1A_TX_DP[1]	L43	PCIEX3	O
724	PE1A_TX_DP[2]	K44	PCIEX3	O
725	PE1A_TX_DP[3]	L45	PCIEX3	O
726	PE1B_RX_DN[4]	J53	PCIEX3	I
727	PE1B_RX_DN[5]	K54	PCIEX3	I
728	PE1B_RX_DN[6]	J57	PCIEX3	I
729	PE1B_RX_DN[7]	K56	PCIEX3	I
730	PE1B_RX_DP[4]	L53	PCIEX3	I
731	PE1B_RX_DP[5]	M54	PCIEX3	I

732	PE1B_RX_DP[6]	L57	PCIEX3	I
733	PE1B_RX_DP[7]	M56	PCIEX3	I
734	PE1B_TX_DN[4]	H46	PCIEX3	O
735	PE1B_TX_DN[5]	J47	PCIEX3	O
736	PE1B_TX_DN[6]	H48	PCIEX3	O
737	PE1B_TX_DN[7]	J49	PCIEX3	O
738	PE1B_TX_DP[4]	K46	PCIEX3	O
739	PE1B_TX_DP[5]	L47	PCIEX3	O
740	PE1B_TX_DP[6]	K48	PCIEX3	O
741	PE1B_TX_DP[7]	L49	PCIEX3	O
742	PE2A_RX_DN[0]	L55	PCIEX3	I
743	PE2A_RX_DN[1]	T54	PCIEX3	I
744	PE2A_RX_DN[2]	T56	PCIEX3	I
745	PE2A_RX_DN[3]	U55	PCIEX3	I
746	PE2A_RX_DP[0]	N55	PCIEX3	I
747	PE2A_RX_DP[1]	V54	PCIEX3	I
748	PE2A_RX_DP[2]	V56	PCIEX3	I
749	PE2A_RX_DP[3]	W55	PCIEX3	I
750	PE2A_TX_DN[0]	AN49	PCIEX3	O
751	PE2A_TX_DN[1]	AM50	PCIEX3	O
752	PE2A_TX_DN[2]	AN51	PCIEX3	O
753	PE2A_TX_DN[3]	AM52	PCIEX3	O
754	PE2A_TX_DP[0]	AR49	PCIEX3	O
755	PE2A_TX_DP[1]	AP50	PCIEX3	O
756	PE2A_TX_DP[2]	AR51	PCIEX3	O
757	PE2A_TX_DP[3]	AP52	PCIEX3	O
758	PE2B_RX_DN[4]	AB54	PCIEX3	I
759	PE2B_RX_DN[5]	AB56	PCIEX3	I
760	PE2B_RX_DN[6]	AC55	PCIEX3	I
761	PE2B_RX_DN[7]	AE57	PCIEX3	I
762	PE2B_RX_DP[4]	AD54	PCIEX3	I
763	PE2B_RX_DP[5]	AD56	PCIEX3	I
764	PE2B_RX_DP[6]	AE55	PCIEX3	I
765	PE2B_RX_DP[7]	AF58	PCIEX3	I
766	PE2B_TX_DN[4]	AG53	PCIEX3	O
767	PE2B_TX_DN[5]	AH54	PCIEX3	O
768	PE2B_TX_DN[6]	AN53	PCIEX3	O
769	PE2B_TX_DN[7]	AP54	PCIEX3	O
770	PE2B_TX_DP[4]	AJ53	PCIEX3	O
771	PE2B_TX_DP[5]	AK54	PCIEX3	O
772	PE2B_TX_DP[6]	AR53	PCIEX3	O
773	PE2B_TX_DP[7]	AT54	PCIEX3	O
774	PE2C_RX_DN[10]	AJ57	PCIEX3	I
775	PE2C_RX_DN[11]	AR57	PCIEX3	I
776	PE2C_RX_DN[8]	AH56	PCIEX3	I
777	PE2C_RX_DN[9]	AK58	PCIEX3	I
778	PE2C_RX_DP[10]	AL57	PCIEX3	I
779	PE2C_RX_DP[11]	AU57	PCIEX3	I
780	PE2C_RX_DP[8]	AK56	PCIEX3	I

781	PE2C_RX_DP[9]	AM58	PCIEX3	I
782	PE2C_TX_DN[10]	AY54	PCIEX3	O
783	PE2C_TX_DN[11]	AW51	PCIEX3	O
784	PE2C_TX_DN[8]	AV52	PCIEX3	O
785	PE2C_TX_DN[9]	AW53	PCIEX3	O
786	PE2C_TX_DP[10]	BB54	PCIEX3	O
787	PE2C_TX_DP[11]	BA51	PCIEX3	O
788	PE2C_TX_DP[8]	AY52	PCIEX3	O
789	PE2C_TX_DP[9]	BA53	PCIEX3	O
790	PE2D_RX_DN[12]	AT58	PCIEX3	I
791	PE2D_RX_DN[13]	AP56	PCIEX3	I
792	PE2D_RX_DN[14]	AY58	PCIEX3	I
793	PE2D_RX_DN[15]	AY56	PCIEX3	I
794	PE2D_RX_DP[12]	AV58	PCIEX3	I
795	PE2D_RX_DP[13]	AT56	PCIEX3	I
796	PE2D_RX_DP[14]	BA57	PCIEX3	I
797	PE2D_RX_DP[15]	BB56	PCIEX3	I
798	PE2D_TX_DN[12]	AV50	PCIEX3	O
799	PE2D_TX_DN[13]	AW49	PCIEX3	O
800	PE2D_TX_DN[14]	AV48	PCIEX3	O
801	PE2D_TX_DN[15]	AW47	PCIEX3	O
802	PE2D_TX_DP[12]	AY50	PCIEX3	O
803	PE2D_TX_DP[13]	BA49	PCIEX3	O
804	PE2D_TX_DP[14]	AY48	PCIEX3	O
805	PE2D_TX_DP[15]	BA47	PCIEX3	O
806	PE3A_RX_DN[0]	AF44	PCIEX3	I
807	PE3A_RX_DN[1]	AG45	PCIEX3	I
808	PE3A_RX_DN[2]	AF46	PCIEX3	I
809	PE3A_RX_DN[3]	AA49	PCIEX3	I
810	PE3A_RX_DP[0]	AH44	PCIEX3	I
811	PE3A_RX_DP[1]	AJ45	PCIEX3	I
812	PE3A_RX_DP[2]	AH46	PCIEX3	I
813	PE3A_RX_DP[3]	AC49	PCIEX3	I
814	PE3A_TX_DN[0]	H50	PCIEX3	O
815	PE3A_TX_DN[1]	J51	PCIEX3	O
816	PE3A_TX_DN[2]	R47	PCIEX3	O
817	PE3A_TX_DN[3]	P48	PCIEX3	O
818	PE3A_TX_DP[0]	K50	PCIEX3	O
819	PE3A_TX_DP[1]	L51	PCIEX3	O
820	PE3A_TX_DP[2]	U47	PCIEX3	O
821	PE3A_TX_DP[3]	T48	PCIEX3	O
822	PE3B_RX_DN[4]	Y50	PCIEX3	I
823	PE3B_RX_DN[5]	Y52	PCIEX3	I
824	PE3B_RX_DN[6]	AA53	PCIEX3	I
825	PE3B_RX_DN[7]	AA51	PCIEX3	I
826	PE3B_RX_DP[4]	AB50	PCIEX3	I
827	PE3B_RX_DP[5]	AB52	PCIEX3	I
828	PE3B_RX_DP[6]	AC53	PCIEX3	I
829	PE3B_RX_DP[7]	AC51	PCIEX3	I

830	PE3B_TX_DN[4]	P52	PCIEX3	O
831	PE3B_TX_DN[5]	R51	PCIEX3	O
832	PE3B_TX_DN[6]	P50	PCIEX3	O
833	PE3B_TX_DN[7]	R49	PCIEX3	O
834	PE3B_TX_DP[4]	T52	PCIEX3	O
835	PE3B_TX_DP[5]	U51	PCIEX3	O
836	PE3B_TX_DP[6]	T50	PCIEX3	O
837	PE3B_TX_DP[7]	U49	PCIEX3	O
838	PE3C_RX_DN[10]	AF50	PCIEX3	I
839	PE3C_RX_DN[11]	AG49	PCIEX3	I
840	PE3C_RX_DN[8]	AF48	PCIEX3	I
841	PE3C_RX_DN[9]	AG51	PCIEX3	I
842	PE3C_RX_DP[10]	AH50	PCIEX3	I
843	PE3C_RX_DP[11]	AJ49	PCIEX3	I
844	PE3C_RX_DP[8]	AH48	PCIEX3	I
845	PE3C_RX_DP[9]	AJ51	PCIEX3	I
846	PE3C_TX_DN[10]	AA47	PCIEX3	O
847	PE3C_TX_DN[11]	Y46	PCIEX3	O
848	PE3C_TX_DN[8]	P46	PCIEX3	O
849	PE3C_TX_DN[9]	R45	PCIEX3	O
850	PE3C_TX_DP[10]	AC47	PCIEX3	O
851	PE3C_TX_DP[11]	AB46	PCIEX3	O
852	PE3C_TX_DP[8]	T46	PCIEX3	O
853	PE3C_TX_DP[9]	U45	PCIEX3	O
854	PE3D_RX_DN[12]	AG47	PCIEX3	I
855	PE3D_RX_DN[13]	AN47	PCIEX3	I
856	PE3D_RX_DN[14]	AM46	PCIEX3	I
857	PE3D_RX_DN[15]	AN45	PCIEX3	I
858	PE3D_RX_DP[12]	AJ47	PCIEX3	I
859	PE3D_RX_DP[13]	AR47	PCIEX3	I
860	PE3D_RX_DP[14]	AP46	PCIEX3	I
861	PE3D_RX_DP[15]	AR45	PCIEX3	I
862	PE3D_TX_DN[12]	AA45	PCIEX3	O
863	PE3D_TX_DN[13]	Y44	PCIEX3	O
864	PE3D_TX_DN[14]	AC43	PCIEX3	O
865	PE3D_TX_DN[15]	T44	PCIEX3	O
866	PE3D_TX_DP[12]	AC45	PCIEX3	O
867	PE3D_TX_DP[13]	AB44	PCIEX3	O
868	PE3D_TX_DP[14]	AA43	PCIEX3	O
869	PE3D_TX_DP[15]	P44	PCIEX3	O
870	PECI	CG55	PECI	I/O
871	PM_FAST_WAKE_N	AV44	CMOS	I/O
872	PMSYNC	K52	CMOS	I
873	PRDY_N	CU49	CMOS	O
874	PREQ_N	CW49	CMOS	I/O
875	PROC_ID	AB48	NA	O
876	PROCHOT_N	BL51	ODCMOS	I/O
877	PWR_DEBUG_N	AC41	CMOS	I
878	PWRGOOD	BJ53	CMOS	I

879	QPI0_CLKRX_DN	BM58	QPI	I
880	QPI0_CLKRX_DP	BK58	QPI	I
881	QPI0_CLKTX_DN	CF44	QPI	O
882	QPI0_CLKTX_DP	CD44	QPI	O
883	QPI0_DRX_DN[0]	BG51	QPI	I
884	QPI0_DRX_DN[1]	BF52	QPI	I
885	QPI0_DRX_DN[10]	BN55	QPI	I
886	QPI0_DRX_DN[11]	BP54	QPI	I
887	QPI0_DRX_DN[12]	BN53	QPI	I
888	QPI0_DRX_DN[13]	BP52	QPI	I
889	QPI0_DRX_DN[14]	BR51	QPI	I
890	QPI0_DRX_DN[15]	BP50	QPI	I
891	QPI0_DRX_DN[16]	BR49	QPI	I
892	QPI0_DRX_DN[17]	BJ49	QPI	I
893	QPI0_DRX_DN[18]	BP48	QPI	I
894	QPI0_DRX_DN[19]	BR47	QPI	I
895	QPI0_DRX_DN[2]	BG53	QPI	I
896	QPI0_DRX_DN[3]	BG55	QPI	I
897	QPI0_DRX_DN[4]	BH56	QPI	I
898	QPI0_DRX_DN[5]	BH54	QPI	I
899	QPI0_DRX_DN[6]	BH50	QPI	I
900	QPI0_DRX_DN[7]	BF58	QPI	I
901	QPI0_DRX_DN[8]	BG57	QPI	I
902	QPI0_DRX_DN[9]	BP56	QPI	I
903	QPI0_DRX_DP[0]	BJ51	QPI	I
904	QPI0_DRX_DP[1]	BH52	QPI	I
905	QPI0_DRX_DP[10]	BL55	QPI	I
906	QPI0_DRX_DP[11]	BM54	QPI	I
907	QPI0_DRX_DP[12]	BL53	QPI	I
908	QPI0_DRX_DP[13]	BM52	QPI	I
909	QPI0_DRX_DP[14]	BN51	QPI	I
910	QPI0_DRX_DP[15]	BM50	QPI	I
911	QPI0_DRX_DP[16]	BN49	QPI	I
912	QPI0_DRX_DP[17]	BG49	QPI	I
913	QPI0_DRX_DP[18]	BM48	QPI	I
914	QPI0_DRX_DP[19]	BN47	QPI	I
915	QPI0_DRX_DP[2]	BE53	QPI	I
916	QPI0_DRX_DP[3]	BE55	QPI	I
917	QPI0_DRX_DP[4]	BF56	QPI	I
918	QPI0_DRX_DP[5]	BF54	QPI	I
919	QPI0_DRX_DP[6]	BF50	QPI	I
920	QPI0_DRX_DP[7]	BD58	QPI	I
921	QPI0_DRX_DP[8]	BE57	QPI	I
922	QPI0_DRX_DP[9]	BM56	QPI	I
923	QPI0_DTX_DN[0]	BW49	QPI	O
924	QPI0_DTX_DN[1]	BW51	QPI	O
925	QPI0_DTX_DN[10]	CF46	QPI	O
926	QPI0_DTX_DN[11]	BY52	QPI	O
927	QPI0_DTX_DN[12]	CA47	QPI	O

928	QPI0_DTX_DN[13]	CA49	QPI	O
929	QPI0_DTX_DN[14]	CG47	QPI	O
930	QPI0_DTX_DN[15]	CF48	QPI	O
931	QPI0_DTX_DN[16]	CF50	QPI	O
932	QPI0_DTX_DN[17]	CF52	QPI	O
933	QPI0_DTX_DN[18]	CG51	QPI	O
934	QPI0_DTX_DN[19]	CG49	QPI	O
935	QPI0_DTX_DN[2]	BW53	QPI	O
936	QPI0_DTX_DN[3]	BY54	QPI	O
937	QPI0_DTX_DN[4]	BW55	QPI	O
938	QPI0_DTX_DN[5]	BV58	QPI	O
939	QPI0_DTX_DN[6]	BW47	QPI	O
940	QPI0_DTX_DN[7]	BW57	QPI	O
941	QPI0_DTX_DN[8]	BY56	QPI	O
942	QPI0_DTX_DN[9]	BW45	QPI	O
943	QPI0_DTX_DP[0]	BV50	QPI	O
944	QPI0_DTX_DP[1]	BV52	QPI	O
945	QPI0_DTX_DP[10]	CD46	QPI	O
946	QPI0_DTX_DP[11]	CA51	QPI	O
947	QPI0_DTX_DP[12]	BY48	QPI	O
948	QPI0_DTX_DP[13]	BY50	QPI	O
949	QPI0_DTX_DP[14]	CE47	QPI	O
950	QPI0_DTX_DP[15]	CD48	QPI	O
951	QPI0_DTX_DP[16]	CD50	QPI	O
952	QPI0_DTX_DP[17]	CD52	QPI	O
953	QPI0_DTX_DP[18]	CE51	QPI	O
954	QPI0_DTX_DP[19]	CE49	QPI	O
955	QPI0_DTX_DP[2]	BU53	QPI	O
956	QPI0_DTX_DP[3]	BV54	QPI	O
957	QPI0_DTX_DP[4]	BU55	QPI	O
958	QPI0_DTX_DP[5]	BT58	QPI	O
959	QPI0_DTX_DP[6]	BV48	QPI	O
960	QPI0_DTX_DP[7]	BU57	QPI	O
961	QPI0_DTX_DP[8]	BV56	QPI	O
962	QPI0_DTX_DP[9]	BV46	QPI	O
963	QPI1_CLKRX_DN	CL53	QPI	I
964	QPI1_CLKRX_DP	CJ53	QPI	I
965	QPI1_CLKTX_DN	CY54	QPI	I
966	QPI1_CLKTX_DP	DB54	QPI	I
967	QPI1_DRX_DN[0]	CM44	QPI	I
968	QPI1_DRX_DN[1]	CN45	QPI	I
969	QPI1_DRX_DN[10]	CT54	QPI	I
970	QPI1_DRX_DN[11]	CR55	QPI	I
971	QPI1_DRX_DN[12]	CT56	QPI	I
972	QPI1_DRX_DN[13]	CR57	QPI	I
973	QPI1_DRX_DN[14]	CP58	QPI	I
974	QPI1_DRX_DN[15]	CK56	QPI	I
975	QPI1_DRX_DN[16]	CL55	QPI	I
976	QPI1_DRX_DN[17]	CF54	QPI	I

977	QPI1_DRX_DN[18]	CF56	QPI	I
978	QPI1_DRX_DN[19]	CE55	QPI	I
979	QPI1_DRX_DN[2]	CM46	QPI	I
980	QPI1_DRX_DN[3]	CN47	QPI	I
981	QPI1_DRX_DN[4]	CM48	QPI	I
982	QPI1_DRX_DN[5]	CN49	QPI	I
983	QPI1_DRX_DN[6]	CM50	QPI	I
984	QPI1_DRX_DN[7]	CN51	QPI	I
985	QPI1_DRX_DN[8]	CV52	QPI	I
986	QPI1_DRX_DN[9]	CU53	QPI	I
987	QPI1_DRX_DP[0]	CK44	QPI	I
988	QPI1_DRX_DP[1]	CL45	QPI	I
989	QPI1_DRX_DP[10]	CP54	QPI	I
990	QPI1_DRX_DP[11]	CU55	QPI	I
991	QPI1_DRX_DP[12]	CV56	QPI	I
992	QPI1_DRX_DP[13]	CU57	QPI	I
993	QPI1_DRX_DP[14]	CT58	QPI	I
994	QPI1_DRX_DP[15]	CM56	QPI	I
995	QPI1_DRX_DP[16]	CJ55	QPI	I
996	QPI1_DRX_DP[17]	CD54	QPI	I
997	QPI1_DRX_DP[18]	CD56	QPI	I
998	QPI1_DRX_DP[19]	CC55	QPI	I
999	QPI1_DRX_DP[2]	CK46	QPI	I
1000	QPI1_DRX_DP[3]	CL47	QPI	I
1001	QPI1_DRX_DP[4]	CK48	QPI	I
1002	QPI1_DRX_DP[5]	CL49	QPI	I
1003	QPI1_DRX_DP[6]	CK50	QPI	I
1004	QPI1_DRX_DP[7]	CL51	QPI	I
1005	QPI1_DRX_DP[8]	CT52	QPI	I
1006	QPI1_DRX_DP[9]	CR53	QPI	I
1007	QPI1_DTX_DN[0]	DE41	QPI	O
1008	QPI1_DTX_DN[1]	DB42	QPI	O
1009	QPI1_DTX_DN[10]	DD48	QPI	O
1010	QPI1_DTX_DN[11]	CW45	QPI	O
1011	QPI1_DTX_DN[12]	DC49	QPI	O
1012	QPI1_DTX_DN[13]	DD50	QPI	O
1013	QPI1_DTX_DN[14]	CW47	QPI	O
1014	QPI1_DTX_DN[15]	DC51	QPI	O
1015	QPI1_DTX_DN[16]	DD52	QPI	O
1016	QPI1_DTX_DN[17]	CV48	QPI	O
1017	QPI1_DTX_DN[18]	CV46	QPI	O
1018	QPI1_DTX_DN[19]	CV44	QPI	O
1019	QPI1_DTX_DN[2]	CW41	QPI	O
1020	QPI1_DTX_DN[3]	DE43	QPI	O
1021	QPI1_DTX_DN[4]	DB44	QPI	O
1022	QPI1_DTX_DN[5]	CV42	QPI	O
1023	QPI1_DTX_DN[6]	DE45	QPI	O
1024	QPI1_DTX_DN[7]	DB46	QPI	O
1025	QPI1_DTX_DN[8]	CW43	QPI	O

1026	QPI1_DTX_DN[9]	DE47	QPI	O
1027	QPI1_DTX_DP[0]	DC41	QPI	O
1028	QPI1_DTX_DP[1]	DD42	QPI	O
1029	QPI1_DTX_DP[10]	DB48	QPI	O
1030	QPI1_DTX_DP[11]	CU45	QPI	O
1031	QPI1_DTX_DP[12]	DE49	QPI	O
1032	QPI1_DTX_DP[13]	DB50	QPI	O
1033	QPI1_DTX_DP[14]	CU47	QPI	O
1034	QPI1_DTX_DP[15]	DE51	QPI	O
1035	QPI1_DTX_DP[16]	DB52	QPI	O
1036	QPI1_DTX_DP[17]	CT48	QPI	O
1037	QPI1_DTX_DP[18]	CT46	QPI	O
1038	QPI1_DTX_DP[19]	CT44	QPI	O
1039	QPI1_DTX_DP[2]	CU41	QPI	O
1040	QPI1_DTX_DP[3]	DC43	QPI	O
1041	QPI1_DTX_DP[4]	DD44	QPI	O
1042	QPI1_DTX_DP[5]	CT42	QPI	O
1043	QPI1_DTX_DP[6]	DC45	QPI	O
1044	QPI1_DTX_DP[7]	DD46	QPI	O
1045	QPI1_DTX_DP[8]	CU43	QPI	O
1046	QPI1_DTX_DP[9]	DC47	QPI	O
1047	RESET_N	CR43	CMOS	I
1048	RSVD	CF40		
1049	RSVD	CP40		
1050	RSVD	R41		
1051	RSVD	M40		
1052	RSVD	AV46		
1053	RSVD	N41		
1054	RSVD	CU51		
1055	RSVD	CW51		
1056	RSVD	B54		
1057	RSVD	F58		
1058	RSVD	E57		
1059	RSVD	DB56		
1060	RSVD	A53		
1061	RSVD	AL55		
1062	RSVD	BD48		
1063	RSVD	AJ55		
1064	RSVD	AY46		
1065	RSVD	CR51		
1066	RSVD	BK44		
1067	RSVD	BN45		
1068	RSVD	BH46		
1069	RSVD	BG43		
1070	RSVD	BE43		
1071	RSVD	BJ45		
1072	RSVD	BH44		
1073	RSVD	BJ43		
1074	RSVD	BM44		

1075	RSVD	BR45		
1076	RSVD	BL43		
1077	RSVD	BP44		
1078	RSVD	BU43		
1079	RSVD	BR43		
1080	RSVD	BD44		
1081	RSVD	BF44		
1082	RSVD	BT44		
1083	RSVD	CA43		
1084	RSVD	BV44		
1085	RSVD	BY44		
1086	RSVD	DE53		
1087	RSVD	C53		
1088	RSVD	F56		
1089	RSVD	D56		
1090	RSVD	K58		
1091	RSVD	H58		
1092	RSVD	AU55		
1093	RSVD	AR55		
1094	RSVD	DE55		
1095	RSVD	DD54		
1096	RSVD	CY58		
1097	RSVD	DA57		
1098	RSVD	BP46		
1099	RSVD	BM46		
1100	RSVD	DC3		
1101	RSVD	CY56		
1102	RSVD	R53		
1103	RSVD	U53		
1104	RSVD	CT50		
1105	RSVD	DA11		
1106	RSVD	BL47		
1107	RSVD	CA53		
1108	RSVD	AM54		
1109	RSVD	AP48		
1110	RSVD	AE45		
1111	RSVD	AA41		
1112	RSVD	Y54		
1113	RSVD	W41		
1114	RSVD	V42		
1115	RSVD	R43		
1116	RSVD	P42		
1117	RSVD	J41		
1118	RSVD	H56		
1119	RSVD	G43		
1120	RSVD	F46		
1121	RSVD	E53		
1122	RSVD	BF48		
1123	RSVD	C41		

1124	RSVD	BH48		
1125	RSVD	AM44		
1126	RSVD	CN43		
1127	RSVD	CL43		
1128	SAFE_MODE_BOOT	BK56	CMOS	I
1129	SKTOCC_N	BU49	NA	O
1130	SOCKET_ID[0]	CP52	CMOS	I
1131	SOCKET_ID[1]	CC53	CMOS	I
1132	SVIDALERT_N	AN43	CMOS	I
1133	SVIDCLK	AU43	ODCMOS	O
1134	SVIDDATA	AR43	ODCMOS	I/O
1135	TCK	CA45	CMOS	I
1136	TDI	CF42	CMOS	I
1137	TDO	CG41	ODCMOS	O
1138	TEST[0]	DB2		
1139	TEST[1]	DB4		
1140	TEST[2]	D2		
1141	TEST[3]	C3		
1142	TEST[4]	BA55		
1143	THERMTRIP_N	BJ47	ODCMOS	O
1144	TMS	BY46	CMOS	I
1145	TRST_N	CV50	CMOS	I
1146	TXT_AGENT	AH52	CMOS	I
1147	TXT_PLTEN	AF52	CMOS	I
1148	VCCD_01	CB16	PWR	
1149	VCCD_01	CB18	PWR	
1150	VCCD_01	CB20	PWR	
1151	VCCD_01	CB22	PWR	
1152	VCCD_01	CB24	PWR	
1153	VCCD_01	CB26	PWR	
1154	VCCD_01	CG17	PWR	
1155	VCCD_01	CG19	PWR	
1156	VCCD_01	CG21	PWR	
1157	VCCD_01	CG23	PWR	
1158	VCCD_01	CG25	PWR	
1159	VCCD_01	CM16	PWR	
1160	VCCD_01	CM18	PWR	
1161	VCCD_01	CM20	PWR	
1162	VCCD_01	CM22	PWR	
1163	VCCD_01	CM24	PWR	
1164	VCCD_01	CM26	PWR	
1165	VCCD_01	CU17	PWR	
1166	VCCD_01	CU19	PWR	
1167	VCCD_01	CU21	PWR	
1168	VCCD_01	CU23	PWR	
1169	VCCD_01	CU25	PWR	
1170	VCCD_01	DB16	PWR	
1171	VCCD_01	DB18	PWR	
1172	VCCD_01	DB20	PWR	

1173	VCCD_01	DB22	PWR	
1174	VCCD_01	DB24	PWR	
1175	VCCD_01	DB26	PWR	
1176	VCCD_01	DE17	PWR	
1177	VCCD_23	AC15	PWR	
1178	VCCD_23	AC17	PWR	
1179	VCCD_23	AC19	PWR	
1180	VCCD_23	AC21	PWR	
1181	VCCD_23	C11	PWR	
1182	VCCD_23	C13	PWR	
1183	VCCD_23	C21	PWR	
1184	VCCD_23	E15	PWR	
1185	VCCD_23	E17	PWR	
1186	VCCD_23	E19	PWR	
1187	VCCD_23	H12	PWR	
1188	VCCD_23	H14	PWR	
1189	VCCD_23	H16	PWR	
1190	VCCD_23	H18	PWR	
1191	VCCD_23	H20	PWR	
1192	VCCD_23	H22	PWR	
1193	VCCD_23	N11	PWR	
1194	VCCD_23	N13	PWR	
1195	VCCD_23	N15	PWR	
1196	VCCD_23	N17	PWR	
1197	VCCD_23	N19	PWR	
1198	VCCD_23	N21	PWR	
1199	VCCD_23	V14	PWR	
1200	VCCD_23	V16	PWR	
1201	VCCD_23	V18	PWR	
1202	VCCD_23	V20	PWR	
1203	VCCD_23	V22	PWR	
1204	VCCIN	CE41	PWR	
1205	VCCIN	AF42	PWR	
1206	VCCIN	AG23	PWR	
1207	VCCIN	AG27	PWR	
1208	VCCIN	AG29	PWR	
1209	VCCIN	AG33	PWR	
1210	VCCIN	AG35	PWR	
1211	VCCIN	AG39	PWR	
1212	VCCIN	AG41	PWR	
1213	VCCIN	AH42	PWR	
1214	VCCIN	AL17	PWR	
1215	VCCIN	AM42	PWR	
1216	VCCIN	AN11	PWR	
1217	VCCIN	AN17	PWR	
1218	VCCIN	AP10	PWR	
1219	VCCIN	AP12	PWR	
1220	VCCIN	AP14	PWR	
1221	VCCIN	AP16	PWR	

1222	VCCIN	AP2	PWR	
1223	VCCIN	AP4	PWR	
1224	VCCIN	AP6	PWR	
1225	VCCIN	AP8	PWR	
1226	VCCIN	AR1	PWR	
1227	VCCIN	AR11	PWR	
1228	VCCIN	AR13	PWR	
1229	VCCIN	AR15	PWR	
1230	VCCIN	AR17	PWR	
1231	VCCIN	AR3	PWR	
1232	VCCIN	AR5	PWR	
1233	VCCIN	AR7	PWR	
1234	VCCIN	AR9	PWR	
1235	VCCIN	AT10	PWR	
1236	VCCIN	AT12	PWR	
1237	VCCIN	AT14	PWR	
1238	VCCIN	AT16	PWR	
1239	VCCIN	AT2	PWR	
1240	VCCIN	AT4	PWR	
1241	VCCIN	AT42	PWR	
1242	VCCIN	AT6	PWR	
1243	VCCIN	AT8	PWR	
1244	VCCIN	AU1	PWR	
1245	VCCIN	AU11	PWR	
1246	VCCIN	AU13	PWR	
1247	VCCIN	AU15	PWR	
1248	VCCIN	AU17	PWR	
1249	VCCIN	AU3	PWR	
1250	VCCIN	AU5	PWR	
1251	VCCIN	AU7	PWR	
1252	VCCIN	AU9	PWR	
1253	VCCIN	AV10	PWR	
1254	VCCIN	AV12	PWR	
1255	VCCIN	AV14	PWR	
1256	VCCIN	AV16	PWR	
1257	VCCIN	AV2	PWR	
1258	VCCIN	AV4	PWR	
1259	VCCIN	AV6	PWR	
1260	VCCIN	AV8	PWR	
1261	VCCIN	AW1	PWR	
1262	VCCIN	AY42	PWR	
1263	VCCIN	BA1	PWR	
1264	VCCIN	BA11	PWR	
1265	VCCIN	BA13	PWR	
1266	VCCIN	BA15	PWR	
1267	VCCIN	BA17	PWR	
1268	VCCIN	BA3	PWR	
1269	VCCIN	BA5	PWR	
1270	VCCIN	BA7	PWR	

1271	VCCIN	BA9	PWR	
1272	VCCIN	BB10	PWR	
1273	VCCIN	BB12	PWR	
1274	VCCIN	BB14	PWR	
1275	VCCIN	BB16	PWR	
1276	VCCIN	BB2	PWR	
1277	VCCIN	BB4	PWR	
1278	VCCIN	BB6	PWR	
1279	VCCIN	BB8	PWR	
1280	VCCIN	BC1	PWR	
1281	VCCIN	BC11	PWR	
1282	VCCIN	BC13	PWR	
1283	VCCIN	BC15	PWR	
1284	VCCIN	BC17	PWR	
1285	VCCIN	BC3	PWR	
1286	VCCIN	BC5	PWR	
1287	VCCIN	BC7	PWR	
1288	VCCIN	BC9	PWR	
1289	VCCIN	BD10	PWR	
1290	VCCIN	BD12	PWR	
1291	VCCIN	BD14	PWR	
1292	VCCIN	BD16	PWR	
1293	VCCIN	BD2	PWR	
1294	VCCIN	BD4	PWR	
1295	VCCIN	BD42	PWR	
1296	VCCIN	BD6	PWR	
1297	VCCIN	BD8	PWR	
1298	VCCIN	BE1	PWR	
1299	VCCIN	BE11	PWR	
1300	VCCIN	BE13	PWR	
1301	VCCIN	BE15	PWR	
1302	VCCIN	BE17	PWR	
1303	VCCIN	BE3	PWR	
1304	VCCIN	BE5	PWR	
1305	VCCIN	BE7	PWR	
1306	VCCIN	BE9	PWR	
1307	VCCIN	BG1	PWR	
1308	VCCIN	BH10	PWR	
1309	VCCIN	BH12	PWR	
1310	VCCIN	BH14	PWR	
1311	VCCIN	BH16	PWR	
1312	VCCIN	BH2	PWR	
1313	VCCIN	BH4	PWR	
1314	VCCIN	BH42	PWR	
1315	VCCIN	BH6	PWR	
1316	VCCIN	BH8	PWR	
1317	VCCIN	BJ1	PWR	
1318	VCCIN	BJ11	PWR	
1319	VCCIN	BJ13	PWR	

1320	VCCIN	BJ15	PWR	
1321	VCCIN	BJ17	PWR	
1322	VCCIN	BJ3	PWR	
1323	VCCIN	BJ5	PWR	
1324	VCCIN	BJ7	PWR	
1325	VCCIN	BJ9	PWR	
1326	VCCIN	BK10	PWR	
1327	VCCIN	BK12	PWR	
1328	VCCIN	BK14	PWR	
1329	VCCIN	BK16	PWR	
1330	VCCIN	BK2	PWR	
1331	VCCIN	BK4	PWR	
1332	VCCIN	BK6	PWR	
1333	VCCIN	BK8	PWR	
1334	VCCIN	BL1	PWR	
1335	VCCIN	BL11	PWR	
1336	VCCIN	BL13	PWR	
1337	VCCIN	BL15	PWR	
1338	VCCIN	BL17	PWR	
1339	VCCIN	BL3	PWR	
1340	VCCIN	BL5	PWR	
1341	VCCIN	BL7	PWR	
1342	VCCIN	BL9	PWR	
1343	VCCIN	BM10	PWR	
1344	VCCIN	BM12	PWR	
1345	VCCIN	BM14	PWR	
1346	VCCIN	BM16	PWR	
1347	VCCIN	BM2	PWR	
1348	VCCIN	BM4	PWR	
1349	VCCIN	BM42	PWR	
1350	VCCIN	BM6	PWR	
1351	VCCIN	BM8	PWR	
1352	VCCIN	BN11	PWR	
1353	VCCIN	BN13	PWR	
1354	VCCIN	BN15	PWR	
1355	VCCIN	BN17	PWR	
1356	VCCIN	BN3	PWR	
1357	VCCIN	BN5	PWR	
1358	VCCIN	BN7	PWR	
1359	VCCIN	BN9	PWR	
1360	VCCIN	BP10	PWR	
1361	VCCIN	BP16	PWR	
1362	VCCIN	BP42	PWR	
1363	VCCIN	BR17	PWR	
1364	VCCIN	BU17	PWR	
1365	VCCIN	BV42	PWR	
1366	VCCIN	BY18	PWR	
1367	VCCIN	BY20	PWR	
1368	VCCIN	BY22	PWR	

1369	VCCIN	BY24	PWR	
1370	VCCIN	BY26	PWR	
1371	VCCIN	BY30	PWR	
1372	VCCIN	BY34	PWR	
1373	VCCIN	BY36	PWR	
1374	VCCIN	BY38	PWR	
1375	VCCIN	BY40	PWR	
1376	VCCIN	BY42	PWR	
1377	VCCIN_SENSE	BN1	PWR	
1378	VCCIO_IN	CC41	PWR	
1379	VCCPECI	CD42	PWR	
1380	VSS	A23	GND	
1381	VSS	A37	GND	
1382	VSS	A39	GND	
1383	VSS	A41	GND	
1384	VSS	A43	GND	
1385	VSS	A45	GND	
1386	VSS	A47	GND	
1387	VSS	A49	GND	
1388	VSS	A5	GND	
1389	VSS	A51	GND	
1390	VSS	A7	GND	
1391	VSS	AA25	GND	
1392	VSS	AA29	GND	
1393	VSS	AA3	GND	
1394	VSS	AA31	GND	
1395	VSS	AA39	GND	
1396	VSS	AA55	GND	
1397	VSS	AA7	GND	
1398	VSS	AB12	GND	
1399	VSS	AB36	GND	
1400	VSS	AB40	GND	
1401	VSS	AB42	GND	
1402	VSS	AC11	GND	
1403	VSS	AC29	GND	
1404	VSS	AC7	GND	
1405	VSS	AC9	GND	
1406	VSS	AD10	GND	
1407	VSS	AD12	GND	
1408	VSS	AD36	GND	
1409	VSS	AD4	GND	
1410	VSS	AD40	GND	
1411	VSS	AD42	GND	
1412	VSS	AD44	GND	
1413	VSS	AD46	GND	
1414	VSS	AD48	GND	
1415	VSS	AD50	GND	
1416	VSS	AD52	GND	
1417	VSS	AD6	GND	

1418	VSS	AD8	GND	
1419	VSS	AE13	GND	
1420	VSS	AE15	GND	
1421	VSS	AE19	GND	
1422	VSS	AE23	GND	
1423	VSS	AE27	GND	
1424	VSS	AE29	GND	
1425	VSS	AE33	GND	
1426	VSS	AE35	GND	
1427	VSS	AE39	GND	
1428	VSS	AE41	GND	
1429	VSS	AE43	GND	
1430	VSS	AE47	GND	
1431	VSS	AE49	GND	
1432	VSS	AE51	GND	
1433	VSS	AE53	GND	
1434	VSS	AF10	GND	
1435	VSS	AF16	GND	
1436	VSS	AF18	GND	
1437	VSS	AF2	GND	
1438	VSS	AF20	GND	
1439	VSS	AF22	GND	
1440	VSS	AF24	GND	
1441	VSS	AF26	GND	
1442	VSS	AF28	GND	
1443	VSS	AF30	GND	
1444	VSS	AF32	GND	
1445	VSS	AF34	GND	
1446	VSS	AF36	GND	
1447	VSS	AF38	GND	
1448	VSS	AF4	GND	
1449	VSS	AF40	GND	
1450	VSS	AF54	GND	
1451	VSS	AF56	GND	
1452	VSS	AF6	GND	
1453	VSS	AF8	GND	
1454	VSS	AG11	GND	
1455	VSS	AG13	GND	
1456	VSS	AG17	GND	
1457	VSS	AG19	GND	
1458	VSS	AG21	GND	
1459	VSS	AG25	GND	
1460	VSS	AG31	GND	
1461	VSS	AG37	GND	
1462	VSS	AG43	GND	
1463	VSS	AG55	GND	
1464	VSS	AG57	GND	
1465	VSS	AH14	GND	
1466	VSS	AH2	GND	

1467	VSS	AH58	GND	
1468	VSS	AH6	GND	
1469	VSS	AJ11	GND	
1470	VSS	AJ17	GND	
1471	VSS	AK16	GND	
1472	VSS	AK4	GND	
1473	VSS	AK42	GND	
1474	VSS	AK44	GND	
1475	VSS	AK46	GND	
1476	VSS	AK48	GND	
1477	VSS	AK50	GND	
1478	VSS	AK52	GND	
1479	VSS	AK6	GND	
1480	VSS	AL11	GND	
1481	VSS	AL43	GND	
1482	VSS	AL45	GND	
1483	VSS	AL47	GND	
1484	VSS	AL49	GND	
1485	VSS	AL51	GND	
1486	VSS	AL53	GND	
1487	VSS	AM10	GND	
1488	VSS	AM12	GND	
1489	VSS	AM14	GND	
1490	VSS	AM16	GND	
1491	VSS	AM2	GND	
1492	VSS	AM4	GND	
1493	VSS	AM56	GND	
1494	VSS	AM6	GND	
1495	VSS	AM8	GND	
1496	VSS	AN1	GND	
1497	VSS	AN13	GND	
1498	VSS	AN15	GND	
1499	VSS	AN3	GND	
1500	VSS	AN5	GND	
1501	VSS	AN55	GND	
1502	VSS	AN57	GND	
1503	VSS	AN7	GND	
1504	VSS	AN9	GND	
1505	VSS	AP42	GND	
1506	VSS	AP44	GND	
1507	VSS	AP58	GND	
1508	VSS	AT44	GND	
1509	VSS	AT46	GND	
1510	VSS	AT48	GND	
1511	VSS	AT50	GND	
1512	VSS	AT52	GND	
1513	VSS	AU45	GND	
1514	VSS	AU47	GND	
1515	VSS	AU49	GND	

1516	VSS	AU51	GND	
1517	VSS	AU53	GND	
1518	VSS	AV42	GND	
1519	VSS	AV54	GND	
1520	VSS	AV56	GND	
1521	VSS	AW11	GND	
1522	VSS	AW13	GND	
1523	VSS	AW15	GND	
1524	VSS	AW17	GND	
1525	VSS	AW3	GND	
1526	VSS	AW5	GND	
1527	VSS	AW55	GND	
1528	VSS	AW57	GND	
1529	VSS	AW7	GND	
1530	VSS	AW9	GND	
1531	VSS	AY10	GND	
1532	VSS	AY12	GND	
1533	VSS	AY14	GND	
1534	VSS	AY16	GND	
1535	VSS	AY2	GND	
1536	VSS	AY4	GND	
1537	VSS	AY44	GND	
1538	VSS	AY6	GND	
1539	VSS	AY8	GND	
1540	VSS	B10	GND	
1541	VSS	B36	GND	
1542	VSS	B40	GND	
1543	VSS	B52	GND	
1544	VSS	B6	GND	
1545	VSS	BB42	GND	
1546	VSS	BB46	GND	
1547	VSS	BB50	GND	
1548	VSS	BB58	GND	
1549	VSS	BC45	GND	
1550	VSS	BC47	GND	
1551	VSS	BC49	GND	
1552	VSS	BC51	GND	
1553	VSS	BC53	GND	
1554	VSS	BC55	GND	
1555	VSS	BC57	GND	
1556	VSS	BD52	GND	
1557	VSS	BD54	GND	
1558	VSS	BD56	GND	
1559	VSS	BE49	GND	
1560	VSS	BE51	GND	
1561	VSS	BF10	GND	
1562	VSS	BF12	GND	
1563	VSS	BF14	GND	
1564	VSS	BF16	GND	

1565	VSS	BF2	GND	
1566	VSS	BF4	GND	
1567	VSS	BF42	GND	
1568	VSS	BF6	GND	
1569	VSS	BF8	GND	
1570	VSS	BG11	GND	
1571	VSS	BG13	GND	
1572	VSS	BG15	GND	
1573	VSS	BG17	GND	
1574	VSS	BG3	GND	
1575	VSS	BG45	GND	
1576	VSS	BG47	GND	
1577	VSS	BG5	GND	
1578	VSS	BG7	GND	
1579	VSS	BG9	GND	
1580	VSS	BH58	GND	
1581	VSS	BJ55	GND	
1582	VSS	BJ57	GND	
1583	VSS	BK42	GND	
1584	VSS	BK46	GND	
1585	VSS	BK48	GND	
1586	VSS	BK50	GND	
1587	VSS	BK52	GND	
1588	VSS	BK54	GND	
1589	VSS	BL45	GND	
1590	VSS	BL49	GND	
1591	VSS	BL57	GND	
1592	VSS	BN43	GND	
1593	VSS	BN57	GND	
1594	VSS	BP12	GND	
1595	VSS	BP14	GND	
1596	VSS	BP4	GND	
1597	VSS	BP58	GND	
1598	VSS	BP6	GND	
1599	VSS	BP8	GND	
1600	VSS	BR1	GND	
1601	VSS	BR11	GND	
1602	VSS	BR13	GND	
1603	VSS	BR15	GND	
1604	VSS	BR3	GND	
1605	VSS	BR5	GND	
1606	VSS	BR53	GND	
1607	VSS	BR55	GND	
1608	VSS	BR57	GND	
1609	VSS	BR7	GND	
1610	VSS	BR9	GND	
1611	VSS	BT10	GND	
1612	VSS	BT16	GND	
1613	VSS	BT42	GND	

1614	VSS	BT46	GND	
1615	VSS	BT48	GND	
1616	VSS	BT50	GND	
1617	VSS	BT52	GND	
1618	VSS	BT54	GND	
1619	VSS	BT56	GND	
1620	VSS	BU3	GND	
1621	VSS	BU45	GND	
1622	VSS	BU47	GND	
1623	VSS	BU5	GND	
1624	VSS	BU51	GND	
1625	VSS	BV10	GND	
1626	VSS	BV16	GND	
1627	VSS	BW15	GND	
1628	VSS	BW17	GND	
1629	VSS	BW43	GND	
1630	VSS	BW5	GND	
1631	VSS	BW7	GND	
1632	VSS	BY10	GND	
1633	VSS	BY28	GND	
1634	VSS	BY32	GND	
1635	VSS	BY58	GND	
1636	VSS	BY8	GND	
1637	VSS	C33	GND	
1638	VSS	C5	GND	
1639	VSS	C55	GND	
1640	VSS	CA13	GND	
1641	VSS	CA15	GND	
1642	VSS	CA17	GND	
1643	VSS	CA19	GND	
1644	VSS	CA21	GND	
1645	VSS	CA23	GND	
1646	VSS	CA25	GND	
1647	VSS	CA27	GND	
1648	VSS	CA29	GND	
1649	VSS	CA31	GND	
1650	VSS	CA33	GND	
1651	VSS	CA35	GND	
1652	VSS	CA37	GND	
1653	VSS	CA39	GND	
1654	VSS	CA41	GND	
1655	VSS	CA5	GND	
1656	VSS	CA55	GND	
1657	VSS	CA57	GND	
1658	VSS	CB10	GND	
1659	VSS	CB12	GND	
1660	VSS	CB14	GND	
1661	VSS	CB2	GND	
1662	VSS	CB30	GND	

1663	VSS	CB34	GND	
1664	VSS	CB36	GND	
1665	VSS	CB38	GND	
1666	VSS	CB40	GND	
1667	VSS	CB42	GND	
1668	VSS	CB44	GND	
1669	VSS	CB46	GND	
1670	VSS	CB48	GND	
1671	VSS	CB50	GND	
1672	VSS	CB52	GND	
1673	VSS	CB54	GND	
1674	VSS	CB56	GND	
1675	VSS	CC11	GND	
1676	VSS	CC3	GND	
1677	VSS	CC33	GND	
1678	VSS	CC43	GND	
1679	VSS	CC45	GND	
1680	VSS	CC47	GND	
1681	VSS	CC49	GND	
1682	VSS	CC5	GND	
1683	VSS	CC7	GND	
1684	VSS	CC9	GND	
1685	VSS	CD12	GND	
1686	VSS	CD4	GND	
1687	VSS	CD40	GND	
1688	VSS	CD6	GND	
1689	VSS	CD8	GND	
1690	VSS	CE15	GND	
1691	VSS	CE33	GND	
1692	VSS	CE43	GND	
1693	VSS	CE45	GND	
1694	VSS	CE7	GND	
1695	VSS	CF10	GND	
1696	VSS	CF12	GND	
1697	VSS	CF28	GND	
1698	VSS	CF32	GND	
1699	VSS	CG27	GND	
1700	VSS	CG29	GND	
1701	VSS	CG31	GND	
1702	VSS	CG33	GND	
1703	VSS	CG35	GND	
1704	VSS	CG37	GND	
1705	VSS	CG39	GND	
1706	VSS	CG43	GND	
1707	VSS	CG45	GND	
1708	VSS	CG5	GND	
1709	VSS	CG53	GND	
1710	VSS	CG7	GND	
1711	VSS	CH12	GND	

1712	VSS	CH30	GND	
1713	VSS	CH34	GND	
1714	VSS	CH36	GND	
1715	VSS	CH38	GND	
1716	VSS	CH40	GND	
1717	VSS	CH42	GND	
1718	VSS	CH44	GND	
1719	VSS	CH46	GND	
1720	VSS	CH48	GND	
1721	VSS	CH50	GND	
1722	VSS	CH52	GND	
1723	VSS	CH54	GND	
1724	VSS	CH56	GND	
1725	VSS	CJ15	GND	
1726	VSS	CJ3	GND	
1727	VSS	CJ33	GND	
1728	VSS	CJ41	GND	
1729	VSS	CJ43	GND	
1730	VSS	CJ45	GND	
1731	VSS	CJ47	GND	
1732	VSS	CJ49	GND	
1733	VSS	CJ51	GND	
1734	VSS	CJ7	GND	
1735	VSS	CK12	GND	
1736	VSS	CK4	GND	
1737	VSS	CK40	GND	
1738	VSS	CK52	GND	
1739	VSS	CK54	GND	
1740	VSS	CL11	GND	
1741	VSS	CL15	GND	
1742	VSS	CL7	GND	
1743	VSS	CL9	GND	
1744	VSS	CM10	GND	
1745	VSS	CM28	GND	
1746	VSS	CM32	GND	
1747	VSS	CM40	GND	
1748	VSS	CM52	GND	
1749	VSS	CM54	GND	
1750	VSS	CM6	GND	
1751	VSS	CM8	GND	
1752	VSS	CN11	GND	
1753	VSS	CN13	GND	
1754	VSS	CN27	GND	
1755	VSS	CN29	GND	
1756	VSS	CN3	GND	
1757	VSS	CN31	GND	
1758	VSS	CN33	GND	
1759	VSS	CN35	GND	
1760	VSS	CN37	GND	

1761	VSS	CN39	GND	
1762	VSS	CN5	GND	
1763	VSS	CN53	GND	
1764	VSS	CN55	GND	
1765	VSS	CN57	GND	
1766	VSS	CN7	GND	
1767	VSS	CP12	GND	
1768	VSS	CP14	GND	
1769	VSS	CP30	GND	
1770	VSS	CP34	GND	
1771	VSS	CP36	GND	
1772	VSS	CP38	GND	
1773	VSS	CP4	GND	
1774	VSS	CP42	GND	
1775	VSS	CP44	GND	
1776	VSS	CP46	GND	
1777	VSS	CP48	GND	
1778	VSS	CP50	GND	
1779	VSS	CP56	GND	
1780	VSS	CR33	GND	
1781	VSS	CR41	GND	
1782	VSS	CR45	GND	
1783	VSS	CR47	GND	
1784	VSS	CR49	GND	
1785	VSS	CR7	GND	
1786	VSS	CR9	GND	
1787	VSS	CT12	GND	
1788	VSS	CT2	GND	
1789	VSS	CT40	GND	
1790	VSS	CU1	GND	
1791	VSS	CU15	GND	
1792	VSS	CU33	GND	
1793	VSS	CU7	GND	
1794	VSS	CV12	GND	
1795	VSS	CV28	GND	
1796	VSS	CV32	GND	
1797	VSS	CV40	GND	
1798	VSS	CV54	GND	
1799	VSS	CV58	GND	
1800	VSS	CV6	GND	
1801	VSS	CW1	GND	
1802	VSS	CW15	GND	
1803	VSS	CW27	GND	
1804	VSS	CW29	GND	
1805	VSS	CW31	GND	
1806	VSS	CW33	GND	
1807	VSS	CW35	GND	
1808	VSS	CW37	GND	
1809	VSS	CW39	GND	

1810	VSS	CW5	GND	
1811	VSS	CW53	GND	
1812	VSS	CW55	GND	
1813	VSS	CW57	GND	
1814	VSS	CW7	GND	
1815	VSS	CY10	GND	
1816	VSS	CY12	GND	
1817	VSS	CY2	GND	
1818	VSS	CY30	GND	
1819	VSS	CY34	GND	
1820	VSS	CY36	GND	
1821	VSS	CY38	GND	
1822	VSS	CY4	GND	
1823	VSS	CY42	GND	
1824	VSS	CY44	GND	
1825	VSS	CY46	GND	
1826	VSS	CY48	GND	
1827	VSS	CY50	GND	
1828	VSS	CY52	GND	
1829	VSS	CY8	GND	
1830	VSS	D10	GND	
1831	VSS	D24	GND	
1832	VSS	D36	GND	
1833	VSS	D4	GND	
1834	VSS	D40	GND	
1835	VSS	DA27	GND	
1836	VSS	DA3	GND	
1837	VSS	DA35	GND	
1838	VSS	DA41	GND	
1839	VSS	DA43	GND	
1840	VSS	DA45	GND	
1841	VSS	DA47	GND	
1842	VSS	DA49	GND	
1843	VSS	DA51	GND	
1844	VSS	DA53	GND	
1845	VSS	DA55	GND	
1846	VSS	DA9	GND	
1847	VSS	DB12	GND	
1848	VSS	DB34	GND	
1849	VSS	DB40	GND	
1850	VSS	DB58	GND	
1851	VSS	DB6	GND	
1852	VSS	DC5	GND	
1853	VSS	DC53	GND	
1854	VSS	DC55	GND	
1855	VSS	DD10	GND	
1856	VSS	DD12	GND	
1857	VSS	DD34	GND	
1858	VSS	DD38	GND	

1859	VSS	DD40	GND	
1860	VSS	DD6	GND	
1861	VSS	DE15	GND	
1862	VSS	DE35	GND	
1863	VSS	DE7	GND	
1864	VSS	DF12	GND	
1865	VSS	DF40	GND	
1866	VSS	DF42	GND	
1867	VSS	DF44	GND	
1868	VSS	DF46	GND	
1869	VSS	DF48	GND	
1870	VSS	DF50	GND	
1871	VSS	DF52	GND	
1872	VSS	DF8	GND	
1873	VSS	E1	GND	
1874	VSS	E3	GND	
1875	VSS	E39	GND	
1876	VSS	E41	GND	
1877	VSS	F2	GND	
1878	VSS	F30	GND	
1879	VSS	F32	GND	
1880	VSS	F36	GND	
1881	VSS	F4	GND	
1882	VSS	F42	GND	
1883	VSS	F44	GND	
1884	VSS	F48	GND	
1885	VSS	F50	GND	
1886	VSS	G1	GND	
1887	VSS	G23	GND	
1888	VSS	G27	GND	
1889	VSS	G33	GND	
1890	VSS	G35	GND	
1891	VSS	G39	GND	
1892	VSS	G41	GND	
1893	VSS	G45	GND	
1894	VSS	G47	GND	
1895	VSS	G49	GND	
1896	VSS	G5	GND	
1897	VSS	G51	GND	
1898	VSS	G53	GND	
1899	VSS	G57	GND	
1900	VSS	G9	GND	
1901	VSS	H24	GND	
1902	VSS	H26	GND	
1903	VSS	H28	GND	
1904	VSS	H30	GND	
1905	VSS	H32	GND	
1906	VSS	H34	GND	
1907	VSS	H36	GND	

1908	VSS	H40	GND	
1909	VSS	H54	GND	
1910	VSS	H6	GND	
1911	VSS	H8	GND	
1912	VSS	J25	GND	
1913	VSS	J29	GND	
1914	VSS	J3	GND	
1915	VSS	J31	GND	
1916	VSS	J37	GND	
1917	VSS	J5	GND	
1918	VSS	J55	GND	
1919	VSS	J7	GND	
1920	VSS	K10	GND	
1921	VSS	K36	GND	
1922	VSS	K40	GND	
1923	VSS	L29	GND	
1924	VSS	L39	GND	
1925	VSS	L41	GND	
1926	VSS	L5	GND	
1927	VSS	M10	GND	
1928	VSS	M2	GND	
1929	VSS	M36	GND	
1930	VSS	M42	GND	
1931	VSS	M44	GND	
1932	VSS	M46	GND	
1933	VSS	M48	GND	
1934	VSS	M50	GND	
1935	VSS	M52	GND	
1936	VSS	N23	GND	
1937	VSS	N27	GND	
1938	VSS	N29	GND	
1939	VSS	N33	GND	
1940	VSS	N35	GND	
1941	VSS	N37	GND	
1942	VSS	N39	GND	
1943	VSS	N43	GND	
1944	VSS	N45	GND	
1945	VSS	N47	GND	
1946	VSS	N49	GND	
1947	VSS	N5	GND	
1948	VSS	N51	GND	
1949	VSS	N53	GND	
1950	VSS	P10	GND	
1951	VSS	P24	GND	
1952	VSS	P26	GND	
1953	VSS	P28	GND	
1954	VSS	P30	GND	
1955	VSS	P32	GND	
1956	VSS	P34	GND	

1957	VSS	P38	GND	
1958	VSS	P40	GND	
1959	VSS	P54	GND	
1960	VSS	P56	GND	
1961	VSS	R11	GND	
1962	VSS	R25	GND	
1963	VSS	R29	GND	
1964	VSS	R31	GND	
1965	VSS	R39	GND	
1966	VSS	R5	GND	
1967	VSS	R55	GND	
1968	VSS	R9	GND	
1969	VSS	T36	GND	
1970	VSS	T4	GND	
1971	VSS	T42	GND	
1972	VSS	T6	GND	
1973	VSS	T8	GND	
1974	VSS	U29	GND	
1975	VSS	U3	GND	
1976	VSS	U39	GND	
1977	VSS	U41	GND	
1978	VSS	U43	GND	
1979	VSS	U7	GND	
1980	VSS	V10	GND	
1981	VSS	V12	GND	
1982	VSS	V36	GND	
1983	VSS	V44	GND	
1984	VSS	V46	GND	
1985	VSS	V48	GND	
1986	VSS	V50	GND	
1987	VSS	V52	GND	
1988	VSS	W23	GND	
1989	VSS	W27	GND	
1990	VSS	W33	GND	
1991	VSS	W35	GND	
1992	VSS	W39	GND	
1993	VSS	W43	GND	
1994	VSS	W45	GND	
1995	VSS	W47	GND	
1996	VSS	W49	GND	
1997	VSS	W51	GND	
1998	VSS	W53	GND	
1999	VSS	W7	GND	
2000	VSS	Y12	GND	
2001	VSS	Y24	GND	
2002	VSS	Y26	GND	
2003	VSS	Y28	GND	
2004	VSS	Y30	GND	
2005	VSS	Y32	GND	

2006	VSS	Y34	GND	
2007	VSS	Y36	GND	
2008	VSS	Y4	GND	
2009	VSS	Y42	GND	
2010	VSS	Y56	GND	
2011	VSS_VCCIN_SENSE	BP2		